FLUKE ®

123/124

Industrial ScopeMeter®

Service Manual

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SERVICE CENTERS

To locate an authorized service center, visit us on the World Wide Web:

http://www.fluke.com

or call Fluke using any of the phone numbers listed below:

+1-888-993-5853 in U.S.A. and Canada

+31-402-675-200 in Europe

+1-425-446-5500 from other countries

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Chapter 1
Safety Instructions

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1.1 Introduction

Read these pages carefully before beginning to install and use the instrument.

The following paragraphs contain information, cautions and warnings which must be followed to ensure safe operation and to keep the instrument in a safe condition.

Warning

Servicing described in this manual is to be done only by qualified service personnel. To avoid electrical shock, do not service the instrument unless you are qualified to do so.

1.2 Safety Precautions

For the correct and safe use of this instrument it is essential that both operating and service personnel follow generally accepted safety procedures in addition to the safety precautions specified in this manual. Specific warning and caution statements, where they apply, will be found throughout the manual. Where necessary, the warning and caution statements and/or symbols are marked on the instrument.

1.3 Caution and Warning Statements

Caution

Used to indicate correct operating or maintenance procedures to prevent damage to or destruction of the equipment or other property.

Warning

Calls attention to a potential danger that requires correct procedures or practices to prevent personal injury.

1.4 Symbols used in this Manual and on Instrument

	Read the safety information in the Users Manual		DOUBLE INSULATION (Protection Class)
	Equal potential inputs, connected internally		Static sensitive components (black/yellow).
	Live voltage		Recycling information
	Earth		Disposal information
	Conformité Européenne		

1.5 Impaired Safety

Whenever it is likely that safety has been impaired, the instrument must be turned off and disconnected from line power. The matter should then be referred to qualified technicians. Safety is likely to be impaired if, for example, the instrument fails to perform the intended measurements or shows visible damage.

1.6 General Safety Information

Warning

Removing the instrument covers or removing parts, except those to which access can be gained by hand, is likely to expose live parts and accessible terminals which can be dangerous to life.

The instrument shall be disconnected from all voltage sources before it is opened.

Capacitors inside the instrument can hold their charge even if the instrument has been separated from all voltage sources.

Components which are important for the safety of the instrument may only be replaced by components obtained through your local FLUKE organization. These parts are indicated with an asterisk (*) in the List of Replaceable Parts, Chapter 8.

Chapter 2
Characteristics

Title	Page

2.1 Introduction

Performance Characteristics

FLUKE guarantees the properties expressed in numerical values with the stated tolerance. Specified non-tolerance numerical values indicate those that could be nominally expected from the mean of a range of identical ScopeMeter test tools.

Environmental Data

The environmental data mentioned in this manual are based on the results of the manufacturer's verification procedures.

Safety Characteristics

The test tool has been designed and tested in accordance with Standards ANSI/ISA S82.01-1994, EN 61010-1 (1993) (IEC 1010-1), CAN/CSA-C22.2 No.1010.1-92 (including approval), UL3111-1 (including approval) Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory Use. Use of this equipment in a manner not specified by the manufacturer may impair protection provided by the equipment.

2.2 Dual Input Oscilloscope

2.2.1 Vertical

Frequency Response

DC Coupled:	
excluding probes and test leads:	
Fluke 123 (via BB120)	DC to 20 MHz (-3 dB)
Fluke 124 (via BB120)	DC to 40 MHz (-3 dB)
with STL120 1:1 shielded test leads:	DC to 12.5 MHz (-3 dB) DC to 20 MHz (-6 dB)
with VP40 10:1 probe:	
Fluke 123 *(optional accessory)*	DC to 20 MHz (-3 dB)
Fluke 124 *(standard accessory)*	DC to 40 MHz (-3 dB)
AC Coupled (LF roll off):	
excluding probes and test leads	<10 Hz (-3 dB)
with STL120	<10 Hz (-3dB)
with 10:1 10MΩ Probe	<1 Hz (-3 dB)

Rise Time

excluding probes and test leads (Fluke 123)	<17.5 ns
excluding probes and test leads (Fluke 124)	<8.75 ns

Input Impedance

excluding probes and test leads	1 MΩ//12 pF
with BB120	1 MΩ//20 pF
with STL120	1 MΩ//225 pF
with VP40 10:1 Probe	5 MΩ//15.5 pF

Sensitivity 5 mV to 500 V/div

Display Modes	A, -A, B, -B
⚠Max. Input Voltage A and B	
Direct, with test leads, or with VP40 Probe with BB120 (For detailed specifications see “2.8 Safety”)	600 Vrms 300 Vrms
⚠Max. Floating Voltage	
from any terminal to ground	600 Vrms, up to 400Hz
Resolution	8 bit
Vertical Accuracy	±(1% + 0.05 range/div)
Max. Vertical Move	±4 divisions
Max. Base Line Jump	After changing time base or sensitivity
Normal & Single mode	±0.04 divisions (= ±1 pixel)

2.2.2 Horizontal

Scope Modes	Normal, Single, Roll
Ranges	
Normal: equivalent sampling (Fluke 123) equivalent sampling (Fluke 124) real time sampling	 20 ns to 500 ns/div 10 ns to 500 ns/div 1 µs to 5 s/div
Single (real time)	1 µs to 5 s/div
Roll (real time)	1s to 60 s/div
Sampling Rate (for both channels simultaneously)	
Equivalent sampling (repetitive signals)	up to 1.25 GS/s
Real time sampling: 1 µs to 5 ms/div 10 ms to 5 s/div	 25 MS/s 5 MS/s
Time Base Accuracy	
Equivalent sampling Real time sampling	±(0.4% +0.04 time/div) ±(0.1% +0.04 time/div)
Glitch Detection	≥40 ns @ 20 ns to 5 ms/div ≥200 ns @ 10 ms to 60 s/div Glitch detection is always active.
Horizontal Move	10 divisions Trigger point can be positioned anywhere across the screen.

2.2.3 Trigger

Screen Update	Free Run, On Trigger
Source	A, B, EXT EXTernal via optically isolated trigger probe ITP120 *(optional accessory)*

Sensitivity A and B (Fluke 123)

@ DC to 5 MHz	0.5 divisions or 5 mV
@ 25 MHz	1.5 divisions
@ 40 MHz	4 divisions

Sensitivity A and B (Fluke 124)

@ DC to 5 MHz	0.5 divisions or 5 mV
@ 40 MHz	1.5 divisions
@ 60 MHz	4 divisions

Voltage level error	±0.5 div. max.
Slope	Positive, Negative
Video on A	Interlaced video signals only
Modes	Lines, Line Select
Standards	PAL , NTSC, PAL+, SECAM
Polarity	Positive, Negative
Sensitivity	0.6 divisions sync.

2.2.4 Advanced Scope Functions

Display Modes

Normal	Captures up to 40 ns glitches and displays analog-like persistence waveform.
Smooth	Suppresses noise from a waveform.
Envelope	Records and displays the minimum and maximum of waveforms over time.

Auto Set
Continuous fully automatic adjustment of amplitude, time base, trigger levels, trigger gap, and hold-off. Manual override by user adjustment of amplitude, time base, or trigger level.

2.3 Dual Input Meter

The accuracy of all measurements is within ± (% of reading + number of counts) from 18 °C to 28 °C.

Add 0.1x (specific accuracy) for each °C below 18 °C or above 28 °C. For voltage measurements with 10:1 probe, add probe uncertainty +1%.

More than one waveform period must be visible on the screen.

2.3.1 Input A and Input B

DC Voltage (VDC)

Ranges	500 mV, 5V, 50V, 500V, 1250V
Accuracy	±(0.5% +5 counts)
Turnover	±12 counts
Normal Mode Rejection (SMR)	>60 dB @ 50 or 60 Hz ±1%
Common Mode Rejection (CMRR)	>100 dB @ DC >60 dB @ 50, 60, or 400 Hz

Full Scale Reading	5000 counts
Move influence	±6 counts max.

True RMS Voltages (VAC and VAC+DC)

Ranges	500 mV, 5V, 50V, 500V, 1250V
Accuracy for 5 to 100% of range	
DC coupled:	
DC to 60 Hz (VAC+DC)	±(1% +10 counts)
1 Hz to 60 Hz (VAC)	±(1% +10 counts)
AC or DC coupled:	
60 Hz to 20 kHz	±(2.5% +15 counts)
20 kHz to 1 MHz	±(5% +20 counts)
1 MHz to 5 MHz	±(10% +25 counts)
5 MHz to 12.5 MHz	±(30% +25 counts)
5 MHz to 20 MHz	±(30% +25 counts), excluding test leads or probes
AC coupled with 1:1 (shielded) test leads:	
60 Hz (6 Hz with 10:1 probe)	-1.5%
50 Hz (5 Hz with 10:1 probe)	-2%
33 Hz (3.3 Hz with 10:1 probe)	-5%
10 Hz (1 Hz with 10:1 probe)	-30%
DC Rejection (only VAC)	>50 dB
Common Mode Rejection (CMRR)	>100 dB @ DC >60 dB @ 50, 60, or 400 Hz
Full Scale Reading	5000 counts The reading is independent of any signal crest factor.
Move influence	±6 counts max.

Peak

Modes	Max peak, Min peak, or pk-to-pk
Ranges	500 mV, 5V, 50V, 500V, 1250V
Accuracy:	
Max peak or Min peak	5% of full scale
Peak-to-Peak	10% of full scale
Full Scale Reading	500 counts

Frequency (Hz)

Ranges	1Hz, 10Hz, 100Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz, 10 MHz, and 50 MHz (Fluke 123) or 70 MHz (Fluke 124).
Frequency Range for Continuous Autoset	15Hz (1Hz) to 50 MHz

Accuracy:	
@1Hz to 1 MHz	±(0.5% +2 counts)
@1 MHz to 10 MHz	±(1.0% +2 counts)
@10 MHz to 50 MHz (Fluke 123)	±(2.5% +2 counts)
@10 MHz to 70 MHz (Fluke 124) (50 MHz in Autorange)	±(2.5% +2 counts)
Full Scale Reading	10 000 counts

Duty Cycle (DUTY)

Range	2% to 98%
Frequency Range for Continuous Autoset	15Hz (1Hz) to 30 MHz
Accuracy:	
@1Hz to 1 MHz	±(0.5% +2 counts)
@1 MHz to 10 MHz	±(1.0% +2 counts)

Pulse Width (PULSE)

Frequency Range for Continuous Autoset	15Hz (1Hz) to 30 MHz
Accuracy:	
@1Hz to 1 MHz	±(0.5% +2 counts)
@1 MHz to 10 MHz	±(1.0% +2 counts)
@10 MHz to 40 MHz	±(2.5% +2 counts)
Full Scale reading	1000 counts

Amperes (AMP)	with optional current probe
Ranges	same as VDC, VAC, VAC+DC, or PEAK
Scale Factor	1 mV/A, 10 mV/A, 100 mV/A, and 1 V/A
Accuracy	same as VDC, VAC, VAC+DC, or PEAK (add current probe uncertainty)
Temperature (TEMP)	with optional temperature probe
Range	200 °C/div (200 °F/div)
Scale Factor	1 mV/°C and 1 mV/°F
Accuracy	as VDC (add temperature probe uncertainty)

Decibel (dB)

0 dBV	1V
0 dBm (600Ω /50Ω)	1 mW, referenced to 600Ω or 50Ω
dB on	VDC, VAC, or VAC+DC
Full Scale Reading	1000 counts

Crest Factor (CREST)

Range	1 to 10
Accuracy	±(5% +1 count)

Full Scale Reading	100 counts
Phase	
Modes	A to B, B to A
Range	0 to 359 degrees
Accuracy	±(1 degree +1 count)
Resolution	1 degree

2.3.2 Input A

Ohm (Ω)	
Ranges	500Ω, 5 kΩ, 50 kΩ, 500 kΩ, 5 MΩ, 30 MΩ
Accuracy	±(0.6% +5 counts)
Full Scale Reading	
500Ω to 5 MΩ	5000 counts
30 MΩ	3000 counts
Measurement Current	0.5 mA to 50 nA decreases with increasing ranges
Open Circuit Voltage	<4V
Continuity (CONT)	
Beep	30Ω ± 5Ω in 50Ω range
Measurement Current	0.5 mA
Detection of shorts of	≥1 ms
Diode	
Maximum Voltage:	
@0.5 mA	>2.8V
@open circuit	<4V
Accuracy	±(2% +5 counts)
Measurement Current	0.5 mA
Polarity	+ on input A, - on COM
Capacitance (CAP)	
Ranges	50 nF, 500 nF, 5 µF, 50 µF, 500 µF
Accuracy	±(2% +10 counts)
Full Scale Reading	5000 counts
Measurement Current	5 µA to 0.5 mA, increases with increasing ranges
Measurement principle	Dual slope integrating measurement with parasitic serial and parallel resistance cancellation.

2.3.3 Advanced Meter Functions

Zero Set	Set actual value to reference
Fast/Normal/Smooth	
Meter settling time Fast	1s @ 1µs to 10 ms/div
Meter settling time Normal	2s @ 1µs to 10 ms/div
Meter settling time Smooth	10s @ 1µs to 10 ms/div
Touch Hold (on A)	Captures and freezes a stable measurement result. Beeps when stable. Touch Hold works on the main meter reading , with threshholds of 1 Vpp for AC signals and 100mV for DC signals.
TrendPlot	Graphs meter readings of the Min and Max values from 15 s/div (120 seconds) to 2 days/div (16 days) with time and date stamp. Automatic vertical scaling and time compression. Displays the actual and Minimum, Maximum, or average (AVG) reading.
Fixed Decimal Point	Possible by using attenuation keys.

2.4 Cursor Readout (Fluke 124)

Sources	A,B
Single Vertical Line	Average, Min and Max Readout. Average, Min, Max and Time from Start of Readout (in ROLL mode, instrument in HOLD). Min, Max and Time from Start of Readout (in TRENDPLOT mode, instrument in HOLD).
Dual Vertical Lines	Peak-Peak, Time Distance and Reciprocal Time Distance Readout. Average, Min, Max and Time Distance Readout (in ROLL mode, instrument in HOLD).
Dual Horizontal Lines	High, Low and Peak-Peak Readout.
Rise or Fall Time	Transition Time, 0%-Level and 100%-Level Readout (Manual or Auto Leveling: Auto Leveling only possible in Single Channel Mode).
Accuracy	As Oscilloscope Accuracy.

2.5 Miscellaneous

Display	
Size	72 x 72 mm (2.83 x 2.83 in)
Resolution	240 x 240 pixels

Waveform display:	
Vertical	8 divisions of 20 pixels
Horizontal	9.6 divisions of 25 pixels
Backlight	Cold Cathode Fluorescent (CCFL)

⚠Power

External:	via Power Adapter PM8907
Input Voltage	10 to 21V DC
Power	5W typical
Input Connector	5 mm jack
Internal Battery Pack BP120 (Fluke 123):	
Battery Power	Rechargeable Ni-Cd 4.8V
Operating Time	4 hours with bright backlight 4.25 hours with dimmed backlight
Charging Time	5 hours with test tool off 40 hours with test tool on 9 ... 14 hours with refresh cycle
Internal Battery Pack BP130 (Fluke 124):	
Battery Power	Rechargeable Ni-MH 4.8V
Operating Time	6 hours with bright backlight 6.3 hours with dimmed backlight
Charging Time	7 hours with test tool off 60 hours with test tool on 12 ... 19 hours with refresh cycle
Allowable ambient temperature during charging	0 to 45 °C (32 to 113 °F)

Memory

Number of Screen + Setup Memories	
Fluke 123	10
Fluke 124	20

Mechanical

Size	232 x 115 x 50 mm (9.1 x 4.5 x 2 in)
Weight	1.2 kg (2.5 lbs), including battery pack.

Interface	RS-232, optically isolated
To Printer	supports Epson FX, LQ, and HP Deskjet®, Laserjet®, and Postscript Serial via PM9080 (optically isolated RS232 adapter/cable, optional). Parallel via PAC91 (optically isolated print adapter cable, optional).
To PC	Dump and load settings and data. Serial via PM9080 (optically isolated RS232 adapter/cable, optional), using SW90W (FlukeView software for Windows).

2.6 Environmental

Environmental	MIL-PRF-28800F, Class 2
Temperature	
Operating	0 to 50 °C (32 to 122 °F)
Storage	-20 to 60 °C (-4 to 140 °F)
Humidity	
Operating:	
@0 to 10 °C (32 to 50 °F)	noncondensing
@10 to 30 °C (50 to 86 °F)	95%
@30 to 40 °C (86 to 104 °F)	75%
@40 to 50 °C (104 to 122 °F)	45%
Storage:	
@-20 to 60 °C (-4 to 140 °F)	noncondensing
Altitude	
Operating	4.5 km (15 000 feet) Max. Input and Floating Voltage 600 Vrms up to 2 km, linearly derating to 400 Vrms @ 4.5 km
Storage	12 km (40 000 feet)
Vibration (Sinusoidal)	MIL28800F, Class 2, 3.8.4.2, 4.5.5.3.1, Max. 3g
Shock	MIL28800F, Class 2, 3.8.5.1, 4.5.5.4.1, Max. 30g
Fungus Resistance	MIL28800F, Class 3, 3.8.7 & 4.5.6.1
Salt Exposure	MIL28800F, Class 2, 3.8.8.2 & 4.5.6.2.2. Structural parts meet 48 hours 5% salt solution test.
Electromagnetic Compatibility (EMC)	
Emission	EN 50081-1 (1992): EN55022 and EN60555-2
Immunity	EN 50082-2(1992): IEC1000-4-2, -3, -4, -5 (see also Section 2.9, Tables 2-1 to 2-3)

Enclosure Protection	IP51, ref: IEC529

2.7 Service and Maintenance

Calibration Interval	1 Year

2.8 Safety

⚠Designed for measurements on 600 Vrms Category III Installations, Pollution Degree 2, per:

- ANSI/ISA S82.01-1994
- EN61010-1 (1993) (IEC1010-1)
- CAN/CSA-C22.2 No.1010.1-92 (including approval)
- UL3111-1 (including approval)

⚠Max. Input Voltage Input A and B

Direct on input, with leads, with VP40	600 Vrms. For derating see Figure 2-1/2.
With Banana-to-BNC Adapter BB120	300V rms. For derating see Figure 2-1.

⚠Max. Floating Voltage

from any terminal to ground	600 Vrms up to 400Hz

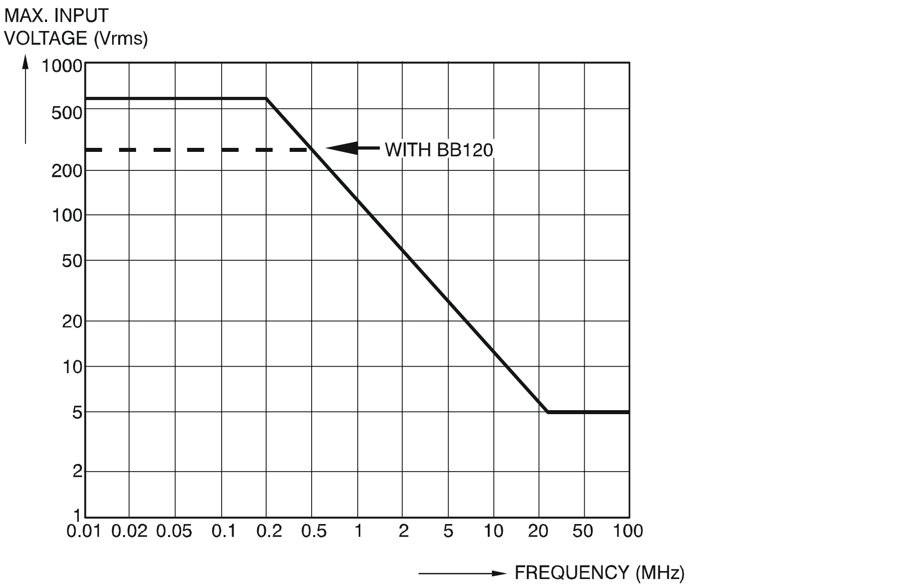


Figure 2-1. Maximum Input Voltage vs Frequency

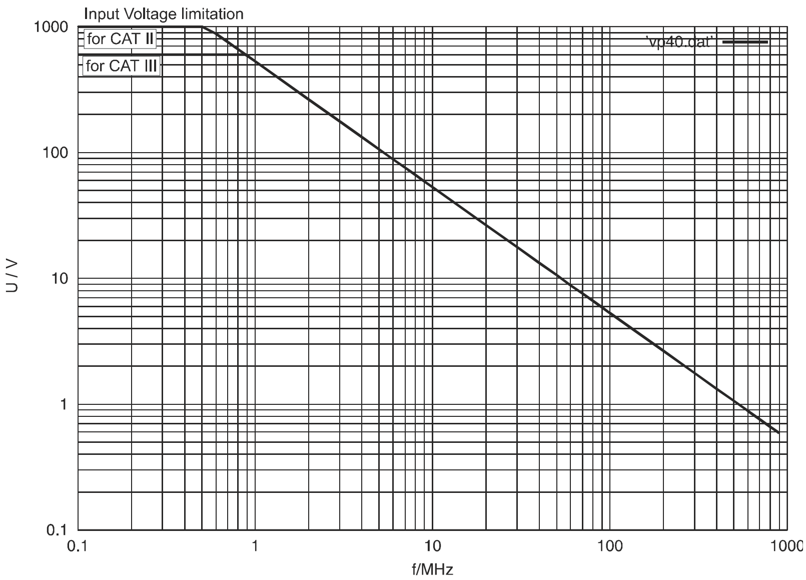


Figure 2-2. Max. Input Voltage v.s. Frequency for VP40 10:1 Voltage Probe

2.9 EMC Immunity

The Fluke 123/124, including standard accessories, conforms with the EEC directive 89/336 for EMC immunity, as defined by IEC1000-4-3, with the addition of tables 2-1 to 2-3.

Trace Disturbance with STL120 See Table 2-1 and Table 2-2.

Table 2-1. No Visible Trace Disturbance

No visible disturbance	E= 3 V/m	E= 10 V/m
Frequency range 10 kHz to 27 MHz	100 mV/div to 500 V/div	500 mV/div to 500 V/div
Frequency range 27 MHz to 1 GHz	100 mV/div to 500 V/div	100 mV/div to 500 V/div

Table 2-2. Trace Disturbance < 10%

Disturbance less than 10% of full scale	E= 3 V/m	E= 10 V/m
Frequency range 10 kHz to 27 MHz	20 mV/div to 50 mV/div	100 mV/div to 200 mV/div
Frequency range 2 MHz to 1 GHz	10 mV/div to 20 mV/div	-

(-): no visible disturbance

Test tool ranges not specified in Table 2-1 and Table 2-2 may have a disturbance of more than 10% of full scale.

Multimeter disturbance See Table 2-3.

- VDC, VAC, and VAC+DC with STL 120 and short ground lead
- OHM, CONT, DIODE, and CAP with STL120 and black test lead to COM

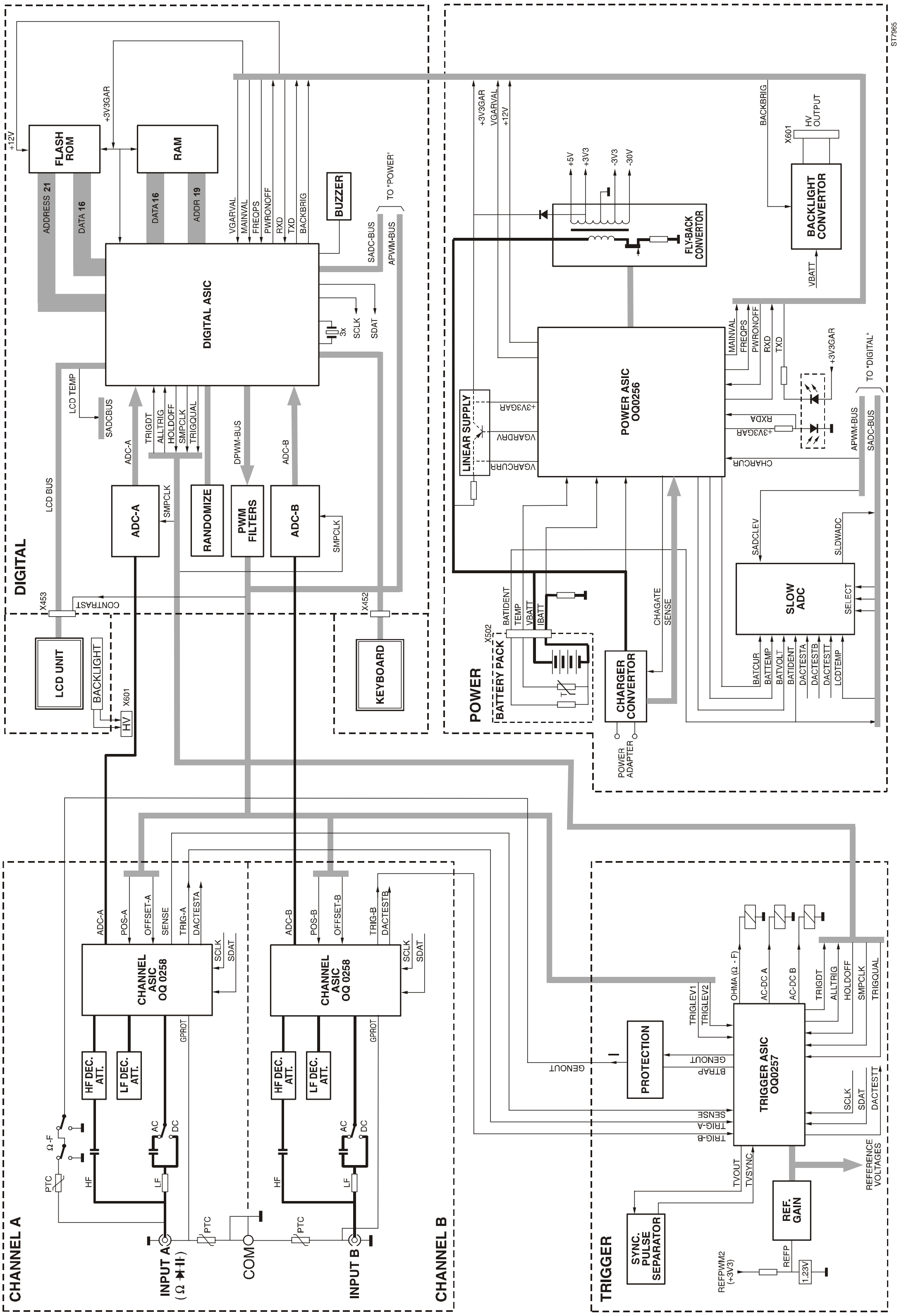
Table 2-3. Multimeter Disturbance < 1%

Disturbance less than 1% of full scale	E= 3 V/m	E= 10 V/m
Frequency range 10 kHz to 27 MHz		
VDC, VAC, VAC+DC	500 mV to 1250V	500 mV to 1250V
OHM, CONT, DIODE	500Ω to 30 MΩ	500Ω to 30 MΩ
CAP	50 nF to 500 μF	50 nF to 500 μF
Frequency range 27 MHz to 1 GHz		
VDC, VAC, VAC+DC	500 mV to 1250V	500 mV to 1250V
OHM, CONT, DIODE	500Ω to 30 MΩ	500Ω to 30 MΩ
CAP	50 nF to 500 μF	50 nF to 500 μF

Test tool ranges not specified in Table 2-3 may have a disturbance of more than 10% of full scale.

Chapter 3
Circuit Descriptions

Title	Page



ST7965.WMF

Figure 3-1. Fluke 123/124 Block Diagram

3.1 Introduction

Section 3.2 describes the functional block diagram shown in Figure 3-1. It provides a quick way to get familiar with the test tool basic build-up.

Section 3.3 describes the principle of operation of the test tool functions in detail, on the basis of the circuit diagrams shown in Figures 9-1 to 9-8.

For all measurements, input signals are applied to the shielded input banana jackets.

Traces and readings are derived from the same input signal samples. So readings are related to the displayed readings.

3.2 Block Diagram

In the overall block diagram Figure 3-1, the test tool is divided in five main blocks. Each block represents a functional part, build up around an Application Specific Integrated Circuit (ASIC). A detailed circuit diagram of each block is shown in Section 9.

See Table 3-1. for an overview of the blocks in which the test tool is broken down, the main block function, the ASIC name, and the applicable circuit diagram.

Table 3-1. Fluke 123/124 Main Blocks

Block	Main Functions	ASIC	Circuit Diagram
CHANNEL A	Input A signal (V-Ω-F) conditioning	C(hannel)-ASIC OQ0258	Figure 9-1
CHANNEL B	Input B signal (V) conditioning	C(hannel)-ASIC OQ0258	Figure 9-2
TRIGGER	Trigger selection and conditioning Current source for resistance, capacitance, continuity, and diode measurements AC/DC input coupling and Ω/F relay control Voltage reference source	T(rigger)-ASIC OQ0257	Figure 9-4
DIGITAL	Analog to Digital Conversion Acquisition of ADC samples Micro controller (µP-ROM-RAM) Keyboard- and LCD control	D(igital)-ASIC HS353063	Figure 9-3 Figure 9-5 Figure 9-5 Figure 9-8
POWER	Power supply, battery charger LCD back light voltage converter Optical interface input	P(ower)-ASIC OQ0256	Figure 9-6 Figure 9-7 Figure 9-6

All circuits, except the LCD unit and the KEYBOARD, are located on one Printed Circuit Board (PCB), called the MAIN PCB.

The ASIC’s are referred to as C-ASIC (Channel ASIC), T-ASIC (Trigger ASIC), P-ASIC (Power ASIC), and D-ASIC (Digital ASIC).

3.2.1 Channel A, Channel B Measurement Circuits

The Channel A and Channel B circuit are similar. The only difference is that Channel A can do all measurements, whereas Channel B does not provide resistance, diode, and capacitance measurements.

Volts, and derived measurements (e.g. current with optional probe)

The input voltage is supplied to the C-ASIC, via the LF and HF path. The C-ASIC converts (attenuates, amplifies) the input signal to a normalized output voltage ADC-A/ADC-B, which is supplied to the Analog to Digital Converters (ADC-A and ADC-B) on the DIGITAL part. The D-ASIC acquires the digital samples to build the trace, and to calculate readings. For the HF and LF attenuation section of the C-ASIC some external components are required: the HF DECade ATTenuator and LF DECade ATTenuator section.

Resistance, continuity, and diode measurements (Input A only)

The T-ASIC supplies a current via the Ω/F relays to the unknown resistance Rx, connected to the Input A and the COM input jacket. The voltage drop across Rx is measured as for voltage measurements.

Capacitance measurements (Input A only)

The T-ASIC supplies a current via the Ω/F relays to the unknown capacitance Cx, connected to the Input A and the COM input jacket. Cx is charged and discharged by this current. The C-ASIC converts the charging time and the discharging time into a pulse width signal. This signal is supplied to the T-ASIC via the C-ASIC trigger output TRIG-A. The T-ASIC shapes and levels the signal, and supplies the resulting pulse width signal ALLTRIG to the D-ASIC. The D-ASIC counts the pulse width and calculates the capacitance reading.

When the capacitance function is selected no other measurement or wave form display is possible. There is only a numeric readout of the capacitance value.

Frequency, pulse width, and duty cycle measurements

The input voltage is measured as described above. From the ADC samples to built the trace, also the frequency, pulse width, and duty cycle of the input signal are calculated.

Miscellaneous

Control of the C-ASIC, e.g. selecting the attenuation factor, is done by the D-ASIC via the SDAT and SCLK serial communication lines.

An offset compensation voltage and a trace position control voltage are provided by the D-ASIC via the APWM bus.

The C-ASIC’s also provide conditioned input voltages on the TRIG-A/TRIG-B line. These voltages can be selected as trigger source by the T-ASIC.

3.2.2 Trigger Circuit

The T ASIC selects one of the possible trigger sources TRIG-A (Input A) or TRIG-B (Input B). For TV triggering the selected trigger source signal is processed via the Sync(hronization) Pulse Separator circuit (TVOUT-TVSYNC lines). Two adjustable trigger levels are supplied by the D-ASIC via the PWM FILTERS (TRIGLEV1 and TRIGLEV2 line). Depending on the selected trigger conditions (- source, - level, - edge, - mode), the T-ASIC generates the final trigger signal TRIGDT, which is supplied to the D-ASIC.

Note

External triggers, supplied via the optical interface RXDA line, are buffered by the P-ASIC, and then supplied to the D-ASIC (RXD signal).

The TRIG-A input is also used for capacitance measurements, as described in Section 3.2.1.

The T-ASIC includes a constant current source for resistance and capacitance measurements. The current is supplied via the GENOUT output and the Ω/F relays to the unknown resistance Rx or capacitance Cx connected to Input A. The SENSE signal senses the voltage across Cx and controls a CLAMP circuit in the T-ASIC. This circuit limits the voltage on Input A at capacitance measurements. The protection circuit prevents the T-ASIC from being damaged by voltages supplied to the input during resistance or capacitance measurements.

For probe adjustment, a voltage generator circuit in the T-ASIC can provide a square wave voltage via the GENOUT output to the Input A connector.

The T-ASIC contains opamps to derive reference voltages from a 1.23V reference source. The gain factors for these opamps are determined by resistors in the REF GAIN circuit. The reference voltages are supplied to various circuits.

The T-ASIC also controls the Channel A and B AC/DC input coupling relays, and the Ω/F relays.

Control data for the T-ASIC are provided by the D-ASIC via the SDAT and SCLK serial communication lines.

3.2.3 Digital Circuit

The D-ASIC includes a micro processor, ADC sample acquisition logic, trigger processing logic, display and keyboard control logic, I/O ports, and various other logic circuits.

The instrument software is stored in the FlashROM, the RAM is used for temporary data storage. The RESET ROM circuit controls the operating mode of the FlashROM (reset, programmable, operational).

For Voltage and Resistance measurements, the conditioned Input A/ Input B voltages are supplied to the ADC-A and ADC-B ADC. The voltages are sampled, and digitized by the ADC's. The output data of the ADC's are acquired and processed by the D-ASIC. For capacitance measurements, the ALLTRIG signal generated by the T-ASIC, is used. The D-ASIC counts the ALLTRIG signal pulse width, which is proportional to the unknown capacitance.

The DPWM-BUS (Digital Pulse Width Modulation) supplies square wave signals with a variable duty cycle to the PWM FILTERS circuit (RC filters). The outgoing APWM-BUS (Analog PWM) provides analog signals of which the amplitude is controlled by the D-ASIC. These voltages are used to control e.g. the trace positions (C-ASIC), the trigger levels (T-ASIC), and the battery charge current (P-ASIC).

In random sampling mode (time base faster than 1 μs/div.), a trace is built-up from several acquisition cycles. During each acquisition, a number of trace samples are placed as pixels in the LCD. The RANDOMIZE circuit takes care that the starting moment of each acquisition cycle (trigger release signal HOLDOFF goes low) is random. This prevents that at each next acquisition the trace is sampled at the same time positions, and that the displayed trace misses samples at some places on the LCD.

The D-ASIC supplies control data and display data to the LCD module. The LCD module is connected to the main board via connector X453. It consists of the LCD, LCD drivers, and a fluorescent back light lamp. As the module is not repairable, no detailed description and diagrams are provided. The back light supply voltage is generated by the back light converter on the POWER part.

The keys of the keyboard are arranged in a matrix. The D-ASIC drives the rows and scans the matrix. The contact pads on the keyboard foil are connected to the main board via connector X452. The ON-OFF key is not included in the matrix, but is sensed by a logic circuit in the D-ASIC, that is active even when the test tool is turned off.

The D-ASIC sends commands to the C-ASICs and T-ASIC via the SCLK and SDAT serial control lines, e.g. to select the required trigger source.

Various I/O lines are provided, e.g. to control the BUZZER and the Slow-ADC (via the SADC bus.

3.2.4 Power Circuit

The test tool can be powered via the power adapter, or by the battery pack.
If the power adapter is connected, it powers the test tool and charges the battery via the CHARGER-CONVERTER circuit. The battery charge current is sensed by sense resistor Rs (signal IBAT). It is controlled by changing the output current of the CHARGER-CONVERTER (control signal CHAGATE).
If no power adapter is connected, the battery pack supplies the VBAT voltage. The VBAT voltage powers the P-ASIC, and is also supplied to the FLY BACK CONVERTER (switched mode power supply).
If the test tool is turned on, the FLY BACK CONVERTER generates supply voltages for various test tool circuits.
The +3V3GAR supply voltage powers the D-ASIC, RAM and ROM. If the test tool is turned off, the battery supplies the +3V3GAR voltage via transistor V569. This transistor is controlled by the P-ASIC. So when the test tool is turned off, the D-ASIC can still control the battery charging process (CHARCURR signal), the real time clock, the on/off key, and the serial RS232 interface (to turn the test tool on).

To monitor and control the battery charging process, the P-ASIC senses and buffers various battery signals, as e.g. temperature (TEMP), voltage (BATVOLT), current (IBAT).

Via the SLOW ADC various analog signals can be measured by the D-ASIC. Involved signals are: battery voltage (BATVOLT), battery type (IDENT), battery temperature (TEMP), battery current (BATCUR) LCD temperature (LCDTEMP, from LCD unit), and 3 test output pins of the C-ASIC’s, and the T-ASIC (DACTEST). The signals are used for control and test purposes.

The BACK LIGHT CONVERTER generates the **400V !** supply voltage for the LCD fluorescent back light lamp. If the lamp is defective a 1.5 kV voltage can be present for 0.2 second maximum. The brightness is controlled by the BACKBRIG signal supplied by the D-ASIC.

Serial communication with a PC or printer is possible via the RS232 optically isolated interface. This interface is also used for external trigger input using the Isolated Trigger Probe. The P-ASIC buffers the received data line (RXDA) and supplies the buffered data (RXD) to the D-ASIC. The transmit data line TXD is directly connected to the D-ASIC.

A linear regulator in the P-ASIC derives a +12V voltage from the power adapter voltage. The +12V is used as programming voltage for the Flash EPROM on the Digital part.

3.2.5 Start-up Sequence, Operating Modes

The test tool sequences through the following steps when power is applied (see also Figure 3-2):

1. The P-ASIC is directly powered by the battery or power adapter voltage VBAT. Initially the Fly Back Converter is off, and the D-ASIC is powered by VBAT via transistor V569 (+3V3GAR).

   If the voltage +3V3GAR is below 3.05V, the P-ASIC keeps its output signal VGARVAL (supplied to the D-ASIC) low, and the D-ASIC will not start up. The test tool is not working, and is in the **Idle mode**.
2. If the voltage +3V3GAR is above 3.05V, the P-ASIC makes the line VGARVAL high, and the D-ASIC will start up. The test tool is operative now. If it is powered by **batteries only**, and **not turned on**, it is in the **Off mode**. In this mode the D-ASIC is active: the real time clock runs, and the ON/OFF key is monitored to see if the test tool will be turned on.
3. If the **power adapter is connected** (P-ASIC output MAINVAL high), **and/or the test tool is turned on**, the embedded D-ASIC program, called mask software, starts up. The mask software checks if valid instrument software is present in the Flash ROM's. If not, the test tool does not start up and the mask software continues running until the test tool is turned off, or the power is removed. This is called the **Mask active mode**. The mask active mode can also be entered by pressing the ^ and > key when turning on the test tool.

   If valid instrument software is present, one of the following modes will become active:

   Charge mode

   The Charge mode is entered when the test tool is **powered by the power adapter, and is turned off**. The FLY-BACK CONVERTER is off. The CHARGER-CONVERTER charges the batteries (if installed).

   Operational & Charge mode

   The Operational & Charge mode is entered when the test tool is **powered by the power adapter, and is turned on**. The FLY-BACK CONVERTER is on, the CHARGER-CONVERTER supplies the primary current. If batteries are installed, they will be charged. In this mode a battery refresh (see below) can be done.

   Operational mode

   The Operational mode is entered when the test tool **is powered by batteries only, and is turned on**. The FLY-BACK CONVERTER is on, the batteries supply the primary current. If the battery voltage (VBAT) drops below 4V when starting up the fly back converter, the Off mode is entered.

Battery Refresh

In the following situations the batteries will need a deep discharge-full charge cycle, called a “refresh”:

- every 50 not-full discharge/charge cycles, or each 3 months. This prevents battery capacity loss due to the memory effect.
- after the battery has been removed, as the test tool does not know the battery status then.

The user will be prompted for this action when he turns the test tool on, directly following the start up screen. A refresh cycle takes 16 hours maximum, depending on the battery status. It can be started via the keyboard (USER OPTIONS, F1, activate refresh) if the test tool is on, and the power adapter is connected. During a refresh, first the battery is completely charged, then it is completely discharged (the test tool is powered by the battery only, and the power adapter must be connected!), and then it is completely charged again.

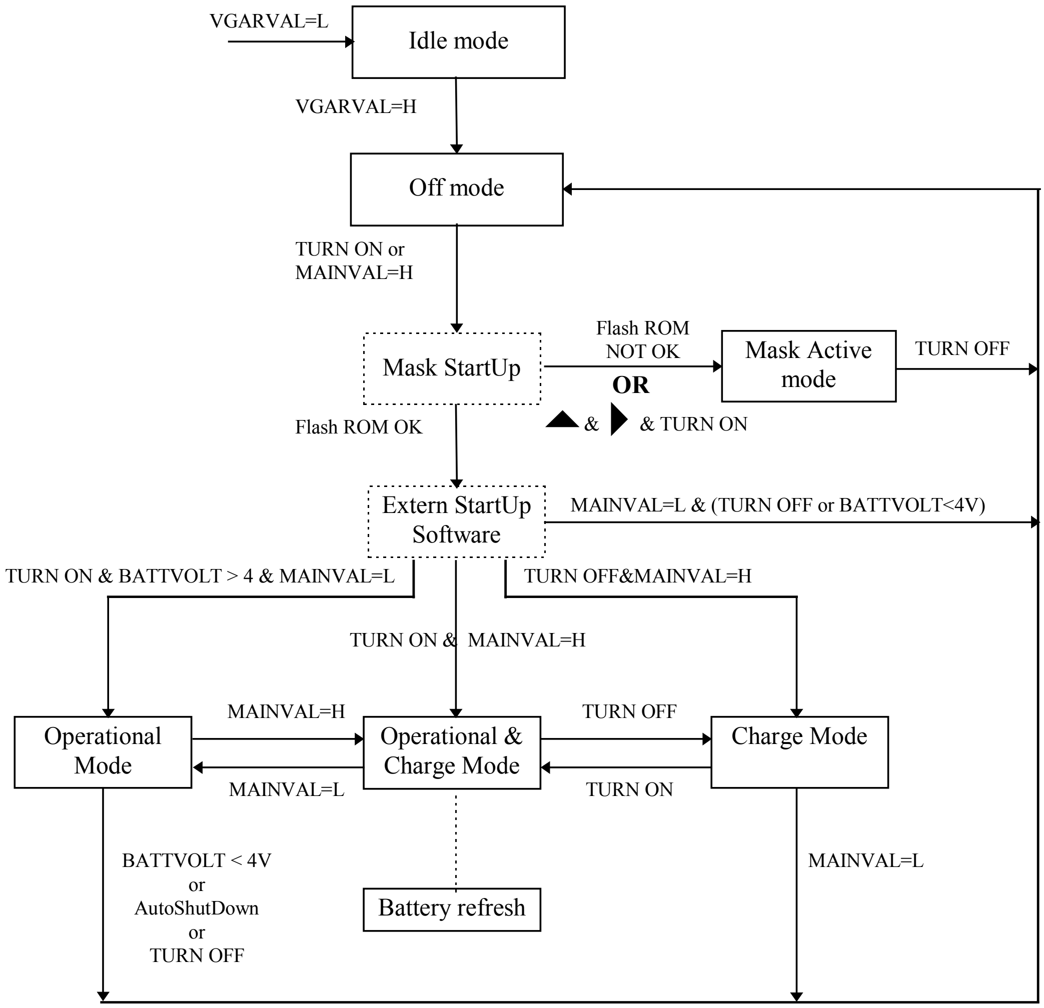


Figure 3-2. Fluke 123/124 Start-up Sequence, Operating Modes

Table 3-2 shows an overview of the test tool operating modes.

Table 3-2. Fluke 123/124 Operating Modes

Mode	Conditions	Remark
Idle mode	No power adapter and no battery	no activity
Off mode	No power adapter connected, battery installed, test tool off	P-ASIC & D-ASIC powered (VBAT & +3V3GAR).
Mask active mode	No valid instrument software, or ^ and > key pressed when turning on	Mask software runs
Charge mode	Power adapter connected and test tool off	Batteries will be charged
Operational & Charge mode	Power adapter connected and test tool on	Test tool operational, and batteries will be charged
Operational mode	No power adapter connected, battery installed, and test tool on	Test tool operational, powered by batteries

3.3 Detailed Circuit Descriptions

3.3.1 Power Circuit

The description below refers to circuit diagram Figure 9-6.

Power Sources , Operating Modes

Figure 3-3 shows a simplified diagram of the power supply and battery charger circuit.

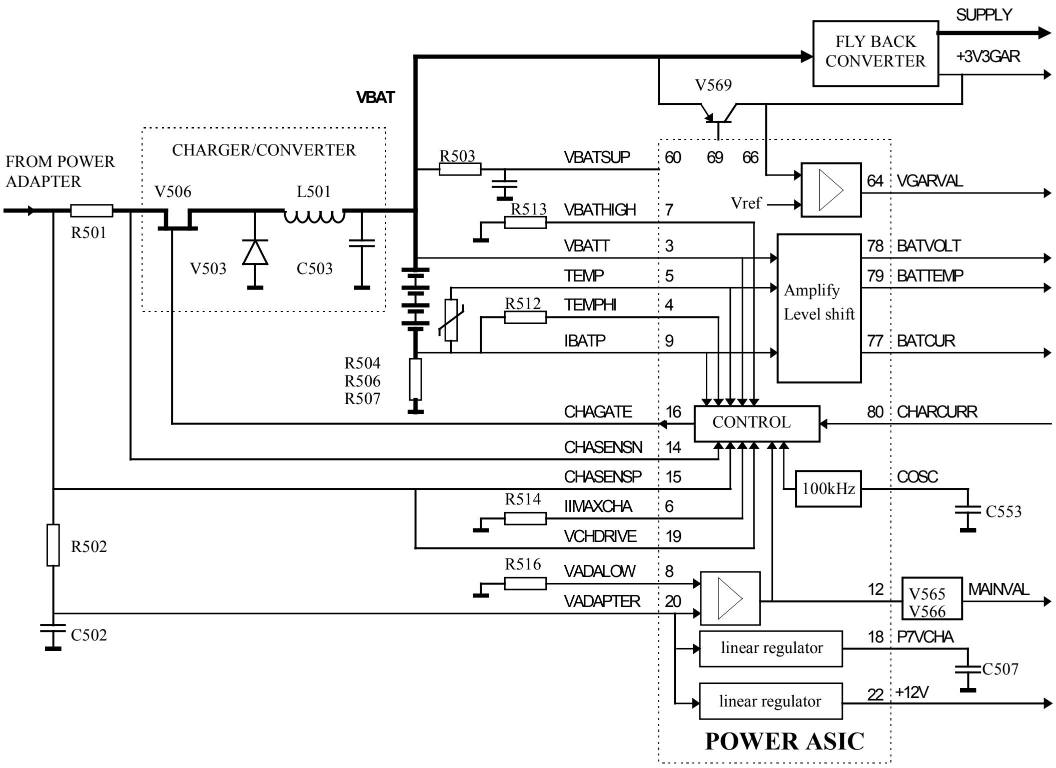


Figure 3-3. Power Supply Block Diagram

As described in Section 3.2.5, the test tool operating mode depends on the connected power source.

The voltage VBAT is supplied either by the power adapter via V506/L501, or by the battery pack. It powers a part of the P-ASIC via R503 to pin 60 (VBATSUP). If the test tool is off, the Fly Back Converter is off, and VBAT powers the D-ASIC via transistor V569 (+3V3GAR). This +3V3GAR voltage is controlled and sensed by the P-ASIC. If it is NOT OK (<3.05V), the output VGARVAL (pin 64) is low. The VGARVAL line is connected to the D-ASIC, and if the line is low, the D-ASIC is inactive: the test tool is in the **Idle mode**. A low VGARVAL line operates as a reset for the D-ASIC.

If VGARVAL is high (+3V3GAR > 3.05V), the D-ASIC becomes active, and the **Off mode** is entered. The D-ASIC monitors the P-ASIC output pin 12 MAINVAL, and the test tool ON/OFF status. By pressing the ON/OFF key, a bit in the D-ASIC, indicating the test tool ON/OFF status is toggled. If neither a correct power adapter voltage is supplied (MAINVAL is low), or the test tool is turned on, the **Off mode** will be maintained.

If a correct power adapter voltage is supplied (MAINVAL high), or if the test tool is turned on, the mask software starts up. The mask software checks if valid instrument software is present. If not, e.g. no instrument firmware is loaded, the mask software will keep running, and the test tool is not operative: the test tool is in the **Mask active** state. For test purposes the mask active mode can also be entered by pressing the ^ and > key when the test tool is turned on.

If valid software is present, one of the three modes **Operational**, **Operational & Charge** or **Charge** will become active. The Charger/Converter circuit is active in the Operational & Charge and in the Charge mode. The Fly back converter is active in the Operational and in the Operational & Charge mode.

Charger/Converter (See Also Figure 3-3.)

The power adapter powers the Charge Control circuit in the P-ASIC via an internal linear regulator. The power adapter voltage is applied to R501. The Charger/Converter circuit controls the battery charge current. If a charged battery pack is installed, VBAT is approximately +4.8V. If no battery pack is installed, VBAT is approximately +15V. The voltage VBAT is supplied to the battery pack, to the P-ASIC, to the Fly Back Converter, and to transistor V569. The FET control signal CHAGATE is a 100 kHz square wave voltage with a variable duty cycle , supplied by the P-ASIC Control circuit. The duty cycle determines the amount of energy loaded into L501/C503. By controlling the voltage VBAT, the battery charge current can be controlled. The various test tool circuits are supplied by the Fly Back Converter, and/or V569.

Required power adapter voltage

The P-ASIC supplies a current to reference resistor R516 (VADALOW pin 8). It compares the voltage on R516 to the power adapter voltage VADAPTER on pin 20 (supplied via R502, and attenuated in the P-ASIC). If the power adapter voltage is below 10V, the P-ASIC output pin 12, and the line MAINVAL, are low. This signal on pin 12 is also supplied to the P-ASIC internal control circuit, which then makes the CHAGATE signal high. As a result FET V506 becomes non-conductive, and the Charger/Converter is off.

Battery charge current control

The actual charge current is sensed via resistors R504-R506-507, and filter R509-C509, on pin 9 of the P-ASIC (IBATP). The sense voltage is supplied to the control circuit. The required charge current information is supplied by the D-ASIC via the CHARCUR line and filter R534-C534 to pin 80. A control loop in the control circuit adjusts the actual charge current to the required value.

The filtered CHARCUR voltage range on pin 80 is 0... 2.7V for a charge current from 0.5A to zero. A voltage of 0V complies to 0.5A (fast charge), 1.5V to 0.2A (top off charge), 2.3V to 0.06A (trickle charge), and 2.7V to 0A (no charge). If the voltage is > 3 Volt, the charger converter is off (V506 permanently non-conductive).

The D-ASIC derives the required charge current value from the battery voltage VBAT. The P-ASIC converts this voltage to an appropriate level and supplies it to output pin 78 (BATVOLT). The D-ASIC measures this voltage via the Slow ADC. The momentary value, and the voltage change as a function of time (-dV/dt), are used as control parameters.

Charging process

If the battery voltage drops below 5.2V, and the battery temperature is between 10 and 45°C, the charge current is set to 0.5A (fast charge). From the battery voltage change -dV/dt the D-ASIC can see when the battery is fully charged, and stop fast charge. Additionally a timer in the D-ASIC limits the fast charge time to 6 hours. After fast charge, a 0.2A top off charge current is supplied for 2 hours. Then a 0.06A trickle charge current is applied for 48 hours maximum. If the battery temperature becomes higher than 50°C, the charge current is set to zero

Battery temperature monitoring

The P-ASIC supplies a current to a NTC resistor in the battery pack (TEMP pin 5 and – of battery). It conditions the voltage on pin 5 and supplies it to output pin 79 BATTEMP. The D-ASIC measures this voltage via the slow ADC. It uses the BATTEMP voltage to decide if fast charge is allowed (10-45°C), or no charge is allowed at all (<10°C, >50°C).

Additionally the temperature is monitored by the P-ASIC. The P-ASIC supplies a current to reference resistor R512 (TEMPHI pin 4), and compares the resulting TEMPHI voltage to the voltage on pin 5 (TEMP). If the battery temperature is too high, the P-ASIC Control circuit will set the charge current to zero, in case the D-ASIC fails to do this.

If the battery temperature monitoring system fails, a bimetal switch in the battery pack interrupts the battery current if the temperature becomes higher then 70 °C.

Two different battery packs are possible: as a standard Fluke 123 is equipped with a Ni-Cd battery, Fluke 124 has a Ni-MH battery that allows a longer operation time. Both instruments will also function on a battery pack different from the standard type. The installed battery type is read by the D-ASIC via BATIDENT/BATIDGAR (pin B5): for Ni-Cd there is 0 Ω between BATIDENT and – of battery, for Ni-MH this is 825 Ω.

Maximum VBAT

The P-ASIC supplies a current to reference resistor R513 (VBATHIGH pin 7). It compares the voltage on R513 to the battery voltage VBAT on pin 3 (after being attenuated in the P-ASIC). The P-ASIC limits the voltage VBAT to 7.4V via its internal Control circuit. This situation arises in case no battery or a defective battery (open) is present.

Charger/Converter input current

This input current is sensed by R501. The P-ASIC supplies a reference current to R514. The P-ASIC compares the voltage drop on R501 (CHASENSP-CHASENSN pin 14 and 15) to the voltage on R514 (IMAXCHA pin 6). It limits the input current (e.g. when loading C503 and C555 just after connecting the power adapter) via its internal Control circuit.

CHAGATE control signal

To make the FET conductive its Vgs (gate-source voltage) must be negative. For that purpose, the CHAGATE voltage must be negative with respect to VCHDRIVE. The P-ASIC voltage VCHDRIVE also limits the swing of the CHAGATE signal to 13V.

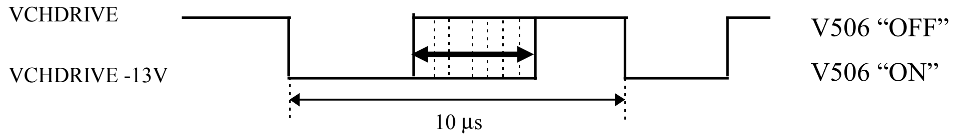


Figure 3-4. CHAGATE Control Voltage

+3V3GAR Voltage

When the test tool is not turned on, the Fly Back Converter does not run. In this situation, the +3V3GAR voltage for the D-ASIC, the FlashROM, and the RAM is supplied via transistor V569. The voltage is controlled by the VGARDRV signal supplied by the P-ASIC (pin 69). The current sense voltage across R580 is supplied to pin 70 (VGARCURR). The voltage +3V3GAR is sensed on pin 66 for regulation. The internal regulator in the P-ASIC regulates the +3V3GAR voltage, and limits the current.

Fly Back Converter

When the test tool is turned on, the D-ASIC makes the PWRONOFF line (P-ASIC pin 62) high. Then the self oscillating Fly Back Converter becomes active. It is started up by the internal 100 kHz oscillator that is also used for the Charger/Converter circuit. First the FLYGATE signal turns FET V554 on (see Figure 3-5), and an increasing current flows in the primary transformer winding to ground, via sense resistor R551. If the voltage FLYSENSP across this resistor exceeds a certain value, the P-ASIC turns FET V554 off. Then a decreasing current flows in the secondary windings to ground. If the windings are “empty” (all energy transferred), the voltage VCOIL sensed by the P-ASIC (pin 52) is zero, and the FLYGATE signal will turn FET V554 on again.

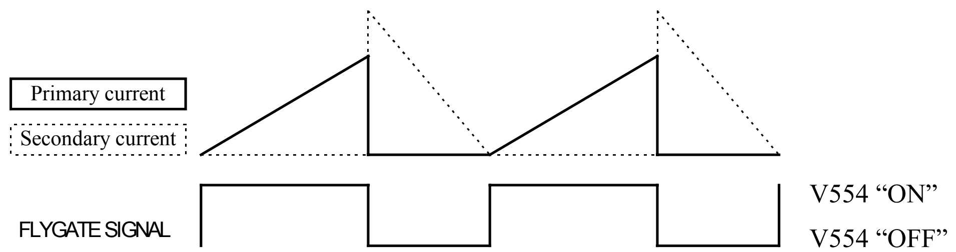


Figure 3-5. Fly-Back Converter Current and Control Voltage

The output voltage is regulated by feeding back a part of the +3V3A output voltage via R552-R553-R554 to pin 54 (VSENS). This voltage is referred to a 1.23V reference voltage. Any deviation of the +3V3A voltage from the required 3.3V changes the current level at which current FET V554 will be switched off. If the output voltage increases, the current level at which V554 is switched off will become lower, and less energy is transferred to the secondary winding. As a result the output voltage will become lower.

An internal current source supplies a current to R559. The resulting voltage is a reference for the maximum allowable primary current (IMAXFLY). The voltage across the sense resistor (FLYSENSP) is compared to the IMAXFLY voltage. If the current exceeds the set limit, FET V554 will be turned off.

Another internal current source supplies a current to R558. This resulting voltage is a reference for the maximum allowable output voltage (VOUTHI). The -3V3A output voltage (M3V3A) is attenuated and level shifted in the P-ASIC, and then compared to the VOUTHI voltage. If the -3V3A voltage exceeds the set limit, FET V554 will be turned off.

The FREQPS control signal is converted to appropriate voltage levels for the FET switch V554 by the BOOST circuit. The voltage VBAT supplies the BOOST circuit power via V553 and R561. The FREQPS signal is also supplied to the D-ASIC, in order to detect if the Fly Back converter is running well.

V551 and C552 limit the voltage on the primary winding of T552 when the FET V554 is turned of. The signal SNUB increases the FLYGATE high level to decreases ON-resistance of V554 (less power dissipation in V554).

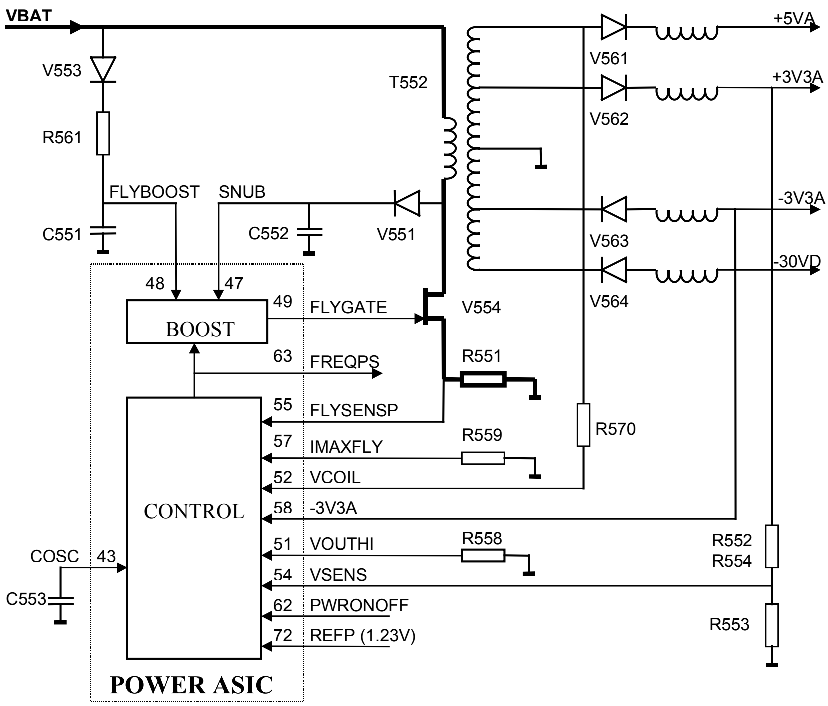


Figure 3-6. Fly-Back Converter Block Diagram

Slow ADC (Refer to Figure 9-7)

The Slow ADC enables the D-ASIC to measure the following signals: BATCUR, BATVOLT, BATTEMP, BATIDENT (Battery current, - voltage, - temperature, - type), DACTEST-A, DACTEST-B, and DACTEST-T (test output of the C-ASIC's and the T-ASIC).

De-multiplexer D531 supplies one of these signals to its output, and to the input of comparator N531 TP536). The D-ASIC supplies the selection control signals SELMUX0-2. The Slow ADC works according to the successive approximation principle. The D-ASIC changes the SADCLEV signal level, and thus the voltage level on pin 3 of the comparator step wise, by changing the duty cycle of the PWM signal SADCLEVD. The comparator output SLOWADC is monitored by the D-ASIC, who knows now if the previous input voltage step caused the comparator output to switch. By increasing the voltage steps, the voltage level can be approximated within the smallest possible step of the SADCLEV voltage. From its set SADCLEVD duty cycle, the D-ASIC knows voltage level of the selected input.

RS232 (Refer to Figure 9-6)

The optical interface is used for two purposes:

- enable serial communication (RS232) between the test tool and a PC or printer
- enable external triggering using the Isolated Trigger Probe ITP120

The received data line RXDA (P-ASIC pin 75) is connected to ground via a 20 kΩ resistor in the P-ASIC.
If no light is received by the light sensitive diode H522, the RXDA line is +200 mV, which corresponds to a “1” (+3V) on the RXD (P-ASIC output pin 76) line.
If light is received, the light sensitive diode will conduct, and the RXDA line goes low (0...-0.6V), which corresponds to a “0” on the RXD line.
The level on the RXDA line is compared by a comparator in the P-ASIC to a 100 mV level. The comparator output is the RXD line, which is supplied to the D-ASIC for communication, and for external triggering.

The D-ASIC controls the transmit data line TXD. If the line is low, diode H521 will emit light.

The supply voltage for the optical interface receive circuit (RXDA), is the +3V3SADC voltage. The +3V3SADC voltage is present if the test tool is turned on, or if the Power Adapter is connected (or both). So if the Power Adapter is present, serial communication is always possible, even when the test tool is off.

Backlight Converter (Refer to Figure 9-7)

The LCD back light is provided by a ∅2.4 mm fluorescent lamp in LCD unit. The back light converter generates the 300-400 Vpp ! supply voltage. The circuit consist of:

- A pulse width modulated (PWM) buck regulator to generate a variable, regulated voltage (V600, V602, L600, C602).
- A zero voltage switched (ZVS) resonant push-pull converter to transform the variable, regulated voltage into a high voltage AC output (V601, T600).

The PWM buck regulator consists of FET V600, V602, L600, C602, and a control circuit in N600. FET V600 is turned on and off by a square wave voltage on the COUT output of N600 pin 14). By changing the duty cycle of this signal, the output on C602 provides a variable, regulated voltage. The turn on edge of the COUT signal is synchronized with each zero detect.

Outputs AOUT and BOUT of N600 provide complementary drive signals for the push-pull FETs V601a/b (dual FET). If V601a conducts, the circuit consisting of the primary winding of transformer T600 and C608, will start oscillating at its resonance frequency. After half a cycle, a zero voltage is detected on pin 9 (ZD) of N600, V601a will be turned off, and V601b is turned on. This process goes on each time a zero is detected. The secondary current is sensed by R600/R604, and fed back to N600 pin 7 and pin 4 for regulation of the PWM buck regulator output voltage. The BACKBRIG signal supplied by the D-ASIC provides a pulse width modulated (variable duty cycle) square wave. By changing the duty cycle of this signal, the average on-resistance of V604 can be changed. This will change the secondary current, and thus the back light intensity. The voltage on the “cold” side of the lamp is limited by V605 and V603. This limits the emission of

electrical interference.
In PCB versions 8 and newer R605 and R606 provide a more reliable startup of the backlight converter.

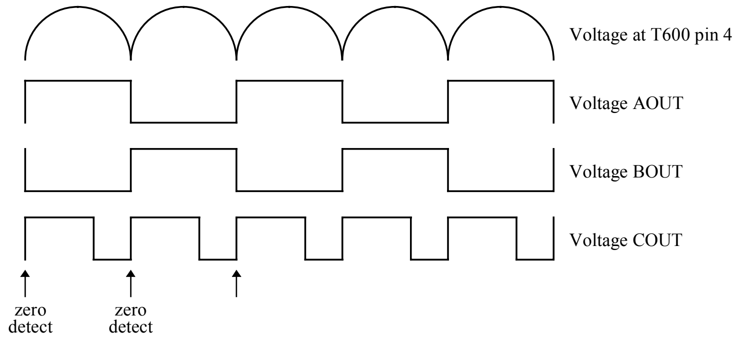


Figure 3-7. Back Light Converter Voltages

3.3.2 Channel A - Channel B Measurement Circuits

The description below refers to circuit diagrams Figure 9-1 and Figure 9-2.

The Channel A and Channel B circuits are almost identical. Both channels can measure voltage, and do time related measurements (frequency, pulse width, etc.). Channel A also provides resistance, continuity, diode, and capacitance measurements.

The Channel A/B circuitry is built-up around a C-ASIC OQ0258. The C-ASIC is placed directly behind the input connector and transforms the input signal to levels that are suitable for the ADC and trigger circuits.

The C-ASIC

Figure 3-8 shows the simplified C-ASIC block diagram. The C-ASIC consists of separate paths for HF and LF signals, an output stage that delivers signals to the trigger and ADC circuits and a control block that allows software control of all modes and adjustments. The transition frequency from the LF-path to the HF-path is approximately 20 kHz, but there is a large overlap.

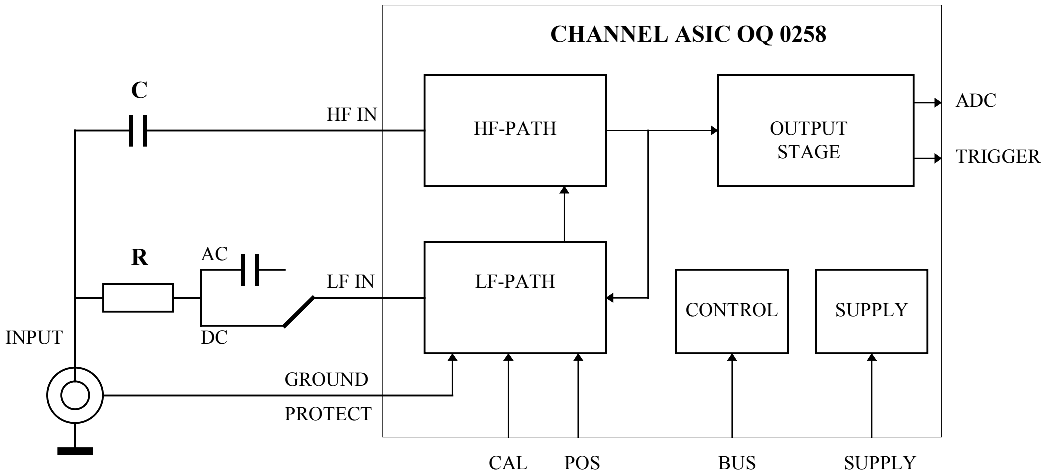


Figure 3-8. C-ASIC Block Diagram

LF input

The LF-input (pin 42) is connected to a LF decade attenuator in voltage mode, or to a high impedance buffer for resistance and capacitance measurements. The LF decade attenuator consists of an amplifier with switchable external feedback resistors R131 to R136. Depending on the selected range the LF attenuation factor which will be set to 1-10-100-1000-10,000. The C-ASIC includes a LF pre-amplifier with switchable gain factors for the 1-2-5 steps.

HF input

The HF component of the input signal is supplied to four external HF capacitive attenuators via C104 and R108. Depending on the required range, the C-ASIC selects and buffers one of the attenuator outputs :1 (HF0), :10 (HF1), :100 (HF2), or :1000 (HF3). By attenuating the HF3 input internally by a factor 10, the C-ASIC can also create a :10000 attenuation factor. Inputs of not selected input buffers are internally shorted. If required, optional FETs V151-V153 can be installed. They will provide an additional input buffer short for the not-selected buffers, to eliminate internal (in the C-ASIC) cross talk. To control the DC bias of the buffers inputs, their output voltage is fed back via an internal feed back resistor and external resistors R115, R111/R120, R112, R113, and-R114. The internal feed back resistor and filter R110/C105 will eliminate HF feed back, to obtain a large HF gain. The C-ASIC includes a HF pre-amplifier with switchable gain factors for the 1-2-5 steps. The C-ASIC also includes circuitry to adjust the gain, and pulse response.

ADC output pin 27

The combined conditioned HF/LF signal is supplied to the ADC output (pin 27) via an internal ADC buffer. The output voltage is 150 mV/division. The MIDADC signal (pin 28), supplied by the ADC, matches the middle of the C-ASIC output voltage swing to the middle if the ADC input voltage swing.

TRIGGER output pin 29

The combined conditioned HF/LF signal is also supplied to the trigger output (pin 29) via an internal trigger buffer. The output voltage is 100 mV/div. This signal (TRIG-A) is supplied to the TRIGGER ASIC for triggering, and time related measurements (See 3.3.4 “Triggering”).

For capacitance measurements the ADC output is not used, but the TRIG-A output pulse length indicates the measured capacitance, see “Capacitance measurements” below.

GPROT input pin 2

PTC (Positive Temperature Coefficient) resistors (R106-R206) are provided between the Input A and Input B shield ground, and the COM input (instrument ground). This prevents damage to the test tool if the various ground inputs are connected to different voltage levels. The voltage across the PTC resistor is supplied via the GPROT input pin 2 to an input buffer. If this voltage exceeds ±200 mV, the ground protect circuit in the C-ASIC makes the DACTEST output (pin 24) high. The DACTEST line output level is read by the D-ASIC via the slow ADC (See 3.3.2 “Power”). The test tool will give a ground error warning.

Because of ground loops, a LF interference voltage can arise across PTC resistor R106 (mainly mains interference when the power adapter is connected). To eliminate this LF interference voltage, it is buffered (also via input GPROT, pin 2), and subtracted from the input signal. Pin 43 (PROTGND) is the ground reference of the input buffer.

CALSIG input pin 36

The reference circuit on the TRIGGER part supplies an accurate +1.23V DC voltage to the CALSIG input pin 36 via R141. This voltage is used for internal calibration of the gain, and the capacitance measurement threshold levels. A reference current Ical is supplied by the T-ASIC via R144 for calibration of the resistance and capacitance measurement function. For ICAL see also Section 3.3.3.

POS input pin 1

The PWM circuit on the Digital part provides an adjustable voltage (0 to 3.3V) to the POS input via R151. The voltage level is used to move the input signal trace on the LCD. The REFN line provides a negative bias voltage via R152, to create the correct voltage swing level on the C-ASIC POS input.

OFFSET input pin 44

The PWM circuit on the Digital part supplies an adjustable voltage (0 to +3.3V) to the OFFSET input via R153. The voltage level is used to compensate the offset in the LF path of the C-ASIC. The REFN line provides a negative bias voltage via R152, to create the correct voltage swing level on the C-ASIC POS input.

DACTEST output pin 24

As described above, the DACTEST output is used for signaling a ground protect error. It can also be used for testing purposes. Furthermore the DACTEST output provides a C-ASIC reset output signal (+1.75V) after a power on.

ADDRESS output pin 23

The output provides a replica of the input voltage to the SENSE line via R165. In capacitance mode, the sense signal controls the CLAMP function in the T-ASIC (See Section 3.3.3).

TRACEROT input pin 31

The TRACEROT signal is supplied by the T-ASIC. It is a triangle sawtooth voltage.

SDAT, SCLK

Control information for the C-ASIC, e.g. selection of the attenuation factor, is sent by the D-ASIC via the SDA data line. The SCL line provides the synchronization clock signal.

Voltage Measurements (Channel A & Channel B)

The following description applies to both Channel A and Channel B.

The input voltage is applied to the HF attenuator inputs of the C-ASIC via C104, and to the LF input of the C-ASIC via R101/R102, AC/DC input coupling relay K171, and R104. The C-ASIC conditions the input voltage to an output voltage of 50 mV/div. This voltage is supplied to the ADC on the Digital part. The ADC output data is read and processed by the D-ASIC, and represented as a numerical reading, and as a graphical trace.

Table 3-3. shows the relation between the reading range (V) and the trace sensitivity (V/div.) The selected trace sensitivity determines the C-ASIC attenuation/gain factor. The reading range is only a readout function, it does not change the hardware range or the wave form display.

Table 3-3. Voltage Ranges And Trace Sensitivity

range	50 mV	50 mV	50 mV	500 mV	500 mV	500 mV	5V	5V
trace ../div	5 mV	10 mV	20 mV	50 mV	100 mV	200 mV	500 mV	1V
range	5V	50V	50V	50V	500V	500V	500V	1250V
trace ../div	2V	5V	10V	20V	50V	100V	200V	500V

During measuring, input voltage measurements, gain measurements, and zero measurements are done. As a result, the voltage supplied to the ADC is a multiplexed (zero, + reference, -reference, input voltage) signal. In ROLL mode however, no gain and zero measurements are done. Now the ADC input voltage includes only the conditioned input voltage.

The input voltage is connected to Input A. The shield of the input is connected to system ground (⊥) via a PTC ground protection resistor. If a voltage is applied between the Input A and Input B ground shield, or between one of these ground shields and the black COM input, the PTC resistor will limit the resulting current. The voltage across the PTC resistor is supplied to the C-ASIC GPROT input, and causes a ground error warning (high voltage level) on output pin 24 (DACTEST).

Resistance Measurements (Channel A)

The unknown resistance Rx is connected to Input A, and the black COM input. The T-ASIC supplies a constant current to Rx via relay contacts K173, and the PTC resistor R172. The voltage across Rx is supplied to a high impedance input buffer in the C-ASIC via the LF input pin 42. The C-ASIC conditions the voltage across Rx to an output voltage of 50 mV/div. This voltage is supplied to the ADC on the Digital part. The ADC data is read and processed by the D-ASIC, and represented as a numerical reading, and a graphical trace in a fixed time base.

Table 3-4 shows the relation between the reading range (Ω), the trace sensitivity (Ω/div.), and the current in Rx. The selected trace sensitivity determines the C-ASIC attenuation/gain factor. The reading range is only a readout function, it does not change the hardware range or the wave form display.

Table 3-4. Ohms Ranges, Trace Sensitivity, and Current

Range	50Ω	500Ω	5kΩ	50 kΩ	500 kΩ	5 MΩ	30 MΩ
Sensitivity ../div	20Ω	200Ω	2 kΩ	20 kΩ	200 kΩ	2 MΩ	10 MΩ
Current in Rx	500 µA	500 µA	50 µA	5 µA	500 nA	50 nA	50 nA

To protect the current source from being damaged by a voltage applied to the input, a PTC resistor R172 and a protection circuit are provided (See Section 3.3.3 “Current Source”).

During measuring, input voltage measurements, gain measurements, and zero measurements are done. As a result, the voltage supplied to the ADC is a multiplexed (zero, + reference, -reference, input voltage) signal.

Capacitance Measurements (Channel A)

The capacitance measurement is based on the equation: C x dV = I x dt. The unknown capacitor Cx is charged with a constant known current. The voltage across Cx increases, and the time lapse between two different known threshold crossings is measured. Thus dV, I and dt are known and the capacitance can be calculated.

The unknown capacitance Cx is connected to the red Input A safety banana socket, and the black COM input. The T-ASIC supplies a constant current to Cx via relay contacts K173, and protection PTC resistor R172. The voltage on Cx is supplied to two comparators in the C-ASIC via the LF input. The threshold levels th_1 and $th_2$of the comparators are fixed (see Figure 3-9). The time lapse between the first and the second threshold crossing depends on the value of Cx. The resulting pulse is supplied to the TRIGGER output pin 29, which is connected to the analog trigger input of the T-ASIC (TRIG-A signal). The T-ASIC adjusts the pulse to an appropriate level, and supplies it to the D-ASIC via its ALLTRIG output. The pulse width is measured and processed by the D-ASIC, and represented on the LCD as numerical reading. There will be no trace displayed.

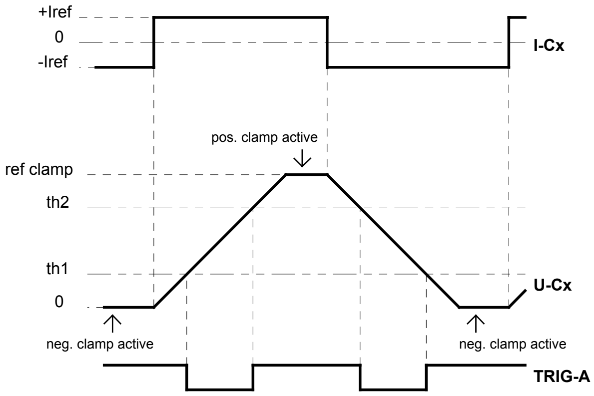


Figure 3-9. Capacitance Measurement

The T-ASIC supplies a positive (charge) and a negative (discharge) current. A measurement cycle starts from a discharged situation (U_{CX}=0) with a charge current. After reaching the first threshold level (th_1) the pulse width measurement is started. The dead zone between start of charge and start of pulse width measurement avoids measurement errors due to a series resistance of Cx.

The pulse width measurement is stopped after crossing the second threshold level (th_2), the completes the first part of the cycle.

Unlimited increase of the capacitor voltage is avoided by the positive clamp in the T-ASIC. The output of the high impedance buffer in the C-ASIC supplies a replica of the voltage across Cx to output pin 23 (ADDRESS). Via R165, this voltage is supplied to a clamp circuit in the T-ASIC (SENSE, pin 59). This clamp circuit limits the positive voltage on Cx to 0.45V.

Now the second part of the measurement is started by reversing the charge current. The capacitor will be discharged in the same way as the charge cycle. The time between passing both threshold levels is measured again. A clamp limits the minimum voltage on Cx to 0V.

Averaging the results of both measurements cancels the effect of a possible parallel resistance, and suppresses the influence of mains interference voltages.

Table 3-5 shows the relation between the capacitance ranges, the charge current and the pulse width at full scale.

Table 3-5. Capacitance Ranges, Current, and Pulse Width

Range	50 nF	500 nF	5000 nF	50 µF	500 µF
Current µA	0.5 µA	5 µA	50 µA	500 µA	500 µA
Pulse width at Full Scale	25 ms	25 ms	25 ms	25 ms	250 ms

To protect the current source if a voltage is applied to the input, a PTC resistor R172, and a protection circuit on the TRIGGER part, are provided (see Section 3.3.3).

Frequency & Pulse Width Measurements

The input voltage is measured as described above. From the ADC samples to built the trace, also the frequency, pulse width, and duty cycle of the input signal are calculated.

Supply Voltages

The +5VA, +3V3A, and -3V3A supply voltages are supplied by the Fly Back Converter on the POWER part. The voltages are present only if the test tool is turned on.

3.3.3 Trigger Circuit

The description refers to circuit diagram Figure 9-4. The trigger section is built up around the T-ASIC OQ0257. It provides the following functions:

- Triggering: trigger source selection, trigger signal conditioning, and generation of trigger information to be supplied to the D-ASIC.
- Current source for resistance and capacitance measurements.
- Voltage reference source: buffering and generation of reference voltages.
- AC/DC relay and Resistance/Capacitance (Ω/F) relay control.

Triggering

Figure 3-10 shows the block diagram of the T-ASIC trigger section.

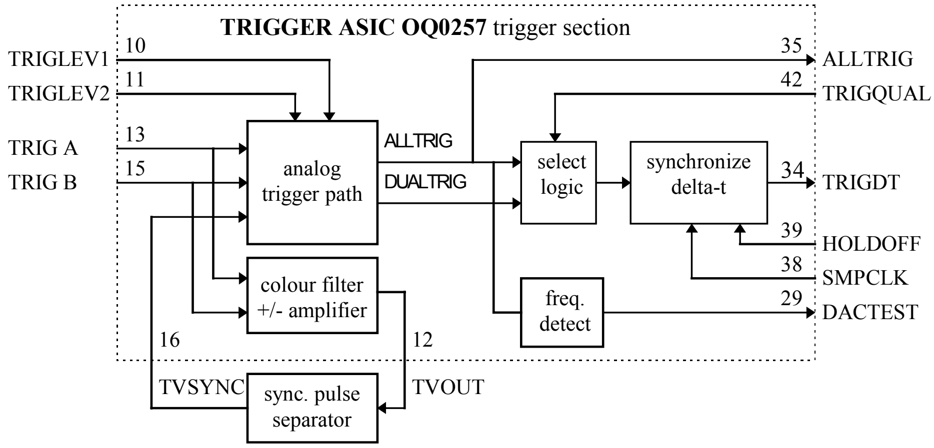


Figure 3-10. T-ASIC Trigger Section Block Diagram

In normal trigger modes (= not TV triggering), the analog trigger path directly uses the Input A (TRIG A) or Input B (TRIG B) signal for triggering.

In the TV trigger mode, the analog trigger path uses the TVSYNC signal for triggering. This signal is the synchronization pulse, derived from the TRIGA or TRIGB composite video signal. The color filter +/- amplify section in the T-ASIC blocks the color information, and amplifies and inverts (if required) the video signal. The TVOUT output signal is supplied to the synchronization pulse separator circuit. This circuit consists of C395, V395 and related parts. The output signal TVSYNC is the synchronization pulse at the appropriate voltage level and amplitude for the T-ASIC analog trigger path.

Note

External triggers provided by the Isolated Trigger Probe to the optical interface are processed directly by the D-ASIC.

The TRIG-A, TRIG-B, or TVSYNC signal, and two trigger level voltages TRIGLEV1 and TRIGLEV2, are supplied to the analog trigger part. The trigger level voltages are, supplied by the PWM section on the Digital part See Section 3.3.4). The TRIGLEV1 voltage is used for triggering on a negative slope of the Input A/B voltage. The TRIGLEV2 voltage is used for triggering on a positive slope of the Input A/B voltage. As the C-ASIC inverts the Input A/B voltage, the TRIGA, TRIGB slopes on the T-ASIC input are inverted! From the selected trigger source signal and the used trigger level voltages, the ALLTRIG and the DUALTRIG trigger signal are derived. The select logic selects which one will be used by the synchronization/delta-T circuit to generate the final trigger. There are three possibilities:

1. Single shot triggering.
   The DUALTRIG signal is supplied to the synchronization/delta-T circuit. The trigger levels TRIGLEV1 and TRIGLEV2 are set just above and below the DC level of the input signal. A trigger is generated when the signal crosses the trigger levels. A trigger will occur on both a positive or a negative glitch. This mode ensures triggering, when the polarity of an expected glitch is not known.
2. Qualified triggering (e.g. TV triggering).
   The ALLTRIG signal is supplied to T-ASIC output pin 35, which is connected to the D-ASIC input pin A16/B15. The D-ASIC derives a qualified trigger signal

TRIGQUAL from ALLTRIG, e.g. on each 10th ALLTRIG pulse a TRIGQUAL pulse is given. The TRIGQUAL is supplied this to the synchronize/delta-T circuit via the select logic.

3. Normal triggering.
   The ALLTRIG signal is supplied to the synchronization/delta-T circuit.

The ALLTRIG signal includes all triggers. It is used by the D-ASIC for signal analysis during AUTOSET.

Traditionally a small trigger gap is applied for each the trigger level. In noisy signals, this small-gap-triggering would lead to unstable displaying of the wave form, if the noise is larger than the gap. The result is that the system will trigger randomly. This problem is solved by increasing the trigger gap (TRIGLEV1 - TRIGLEV2) automatically to 80% (10 to 90%) of the input signal peak-to-peak value. This 80% gap is used in AUTOSET.

Note

The ALLTRIG signal is also used for frequency/pulse width -, and capacitance measurements. Section 3.3.2.

The Synchronize/Delta-t part provides an output pulse TRIGDT. The front edge of this pulse is the real trigger moment. The pulse width is a measure for the time between the trigger moment, and the moment of the first sample after the trigger. This pulse width information is required in random repetitive sampling mode (see below). The HOLDOFF signal, supplied by the D-ASIC, releases the trigger system. The sample clock SMPCLK_B, also provided by the D-ASIC, is used for synchronization.

Real time sampling TRIGDT signal

For time base settings of 1 µs/div and slower, the pixel distance on the LCD is ≥40 ns (1 division is 25 pixels). As the maximum sample rate is 25 MHz, a sample is taken each 40 ns. So the first sample after a trigger can be assigned to the first pixel, and successive samples to each next pixel. So a trace can be built-up from a single period of the input signal.

Random repetitive (equivalent) sampling TRIGDT signal

For time base settings below 1 µs/div, the time between two successive pixels on the screen is smaller than the time between two successive samples. For example at 20 ns/div, the time between two pixels is 20:25=0.8 ns, and the sample distance is 40 ns (sample rate 25 MHz). A number of sweeps must be taken to reconstruct the original signal, see Figure 3-11. As the samples are taken randomly with respect to the trigger moment, the time dt must be known to position the samples on the correct LCD pixel. The TRIGDT signal is a measure for the time between the trigger and the sample moment dt. The pulse duration of the TRIGDT signal is approximately 4 µs...20 µs.

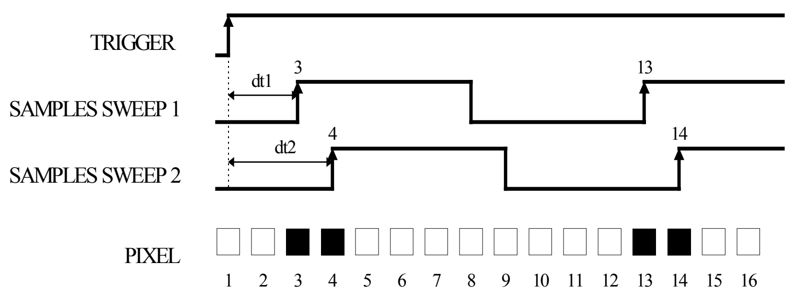


Figure 3-11. Random Repetitive Sampling Mode

DACTEST output

A frequency detector in the T-ASIC monitors the ALLTRIG signal frequency. If the frequency is too high to obtain a reliable transmission to the D-ASIC, the DACTEST output pin 29 will become high. The DACTEST signal is read by the D-ASIC via the slow ADC on the Power part. It and indicates that the D-ASIC cannot use the ALLTRIG signal (e.g. for qualified triggering).

Current Source

A current source in the T-ASIC supplies a DC current to the GENOUT output pin 1. The current is used for resistance and capacitance measurements. It is adjustable in decades between 50 nA and 500 µA depending on the measurement range, and is derived from an external reference current. This reference current is supplied by the REFP reference voltage via R323 and R324 to input REFOHMIN (pin 6).

The SENSE input signal is the buffered voltage on Input A. For capacitance measurements it is supplied to a clamp circuit in the T-ASIC (pin 59). The clamp circuit limits the positive voltage on the unknown capacitance to 0.45V.

The protection circuit prevents the T-ASIC from being damaged by a voltage applied to Input A during resistance or capacitance measurements. If a voltage is applied, a current will flow via PTC resistor R172 (on the Channel A part), V358/V359, V353, V354 to ground. The resulting voltage across the diodes is approximately -2V or +15V. R354/R356, and V356/V357 limit the voltage on the T-ASIC GENOUT output (pin 1). The BOOTSTRAP output signal on pin 3 is the buffered GENOUT signal on pin 1, or the buffered SENSE signal on pin 59. It is supplied to the protection diodes via R352, R353, and to protection transistor V356, to minimize leakage currents.

On the ICAL-output of the T-ASIC (pin 5) a copy of the output current on GENOUT is available. The current is supplied to the Channel A C-ASIC via R144. ICAL shows the same time/temperature drift as the GENOUT measurement current, it can be used for internal calibration of the resistance and capacitance measurement function.

Capacitor C356 is use for hum/noise suppression.

Square Wave Voltage Generator For Probe Adjustment

For probe adjustment, a voltage generator circuit in the T-ASIC can provide a 2.5Vpp, 760Hz, square wave voltage via the GENOUT output pin 1 to the Input A connector. Capacitor C357 is the external timing capacitor for the generator.

Reference Voltage Circuit

This circuit derives several reference voltages from the 1.23V main reference source.

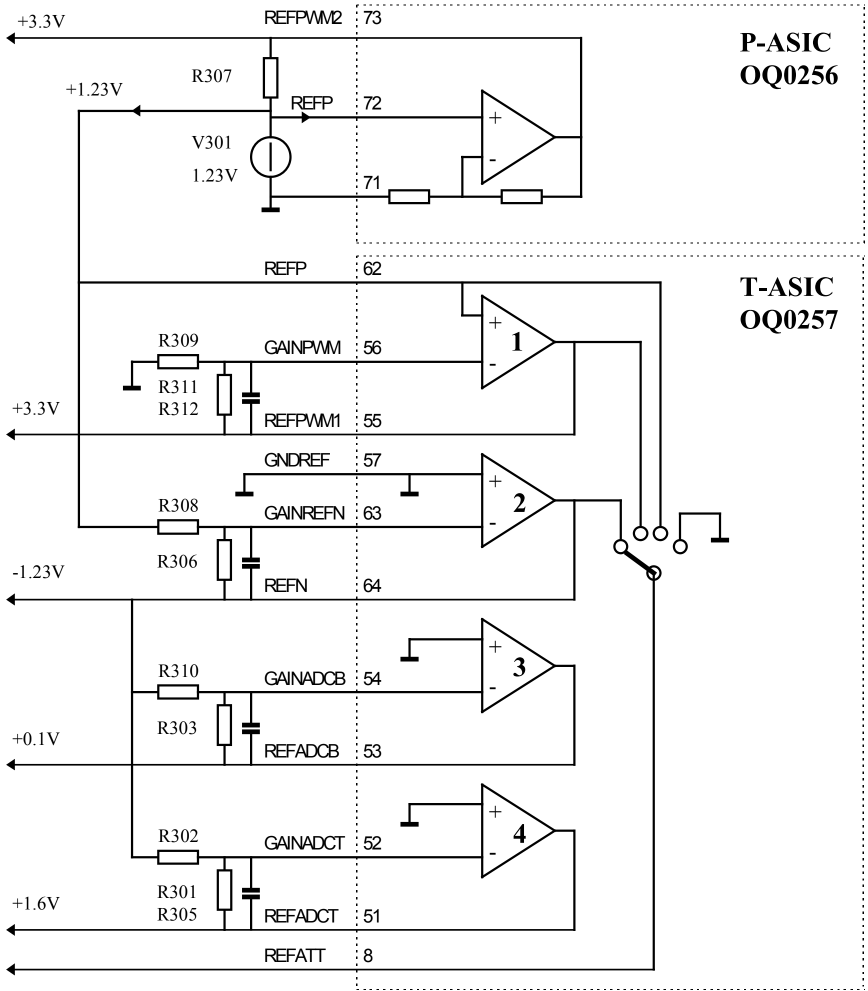


Figure 3-12. Reference Voltage Section

The output of an amplifier in the P-ASIC supplies a current to the +1.23V reference source V301 via R307. The +3.3V REFPWM2 voltage is used as reference for the PWMB outputs of the D-ASIC on the Digital part.

The +1.23V REFP voltage is used as main reference source for the reference circuit. This circuit consists of four amplifiers in the T-ASIC, external gain resistors, and filter capacitors.

Amplifier 1 and connected resistors supply the REFPWM1 reference voltage. This voltage is a reference for the PWMA outputs of the D-ASIC on the Digital section. It is also used as reference voltage for the LCD supply on the LCD unit.

Amplifier 2 and connected resistors supply the -1.23V REFN reference voltage, used for the trigger level voltages TRIGLEV1&2, the C-ASIC POS-A and POS-B voltages, and the C-ASIC OFFSET-A and OFFSET-B voltages. REFN is also the input reference for amplifiers 3 and 4.

Amplifier 3 and 4 and connected resistors supply the REFADCT and REFADCB reference voltages for the ADC's. Both voltages directly influence the gain accuracy of the ADC's.

The T-ASIC can select some of the reference voltages to be output to pin 8 (REFATT). The REFATT voltage is used for internal calibration of the input A and B overall gain.

Tracerot Signal

The T-ASIC generates the TRACEROT signal, used by the C-ASIC's. Control signals TROTRST and TROTCLK are provided by the D-ASIC.

AC/DC Relay and Ω/F Relay Control

The Channel A/B AC/DC relays K171/K271, and the Channel A Ω/F relay K173 are controlled by the T-ASIC output signals ACDCA (pin 22), ACDCB (pin 23) and OHMA (pin 24).

SCLK, SDAT Signals

T-ASIC control data, e.g. for trigger source/mode/edge selection and relay control, are provided by the D-ASIC via the SCLK and SDAT serial control lines..

3.3.4 Digital Circuit and ADC's

Refer to the Fluke 123/124 block diagram Figure 3-1, and circuit diagrams in Figure 9-5 (Digital Circuit) and Figure 9-3 (ADC-section).

The Digital part is built up around the D-ASIC HS353063 (D471A). It provides the following functions:

- ADC data acquisition for traces and numerical readings
- Trigger processing
- Pulse width measurements, e.g. for capacitance measurement function
- Microprocessor, Flash EPROM and RAM control
- Display control
- Keyboard control, ON/OFF control
- Miscellaneous functions, as PWM signal generation, SDA-SCL serial data control, probe detection, Slow ADC control, serial RS232 interface control, buzzer control, etc.

The D-ASIC is permanently powered by the +3V3GAR voltage supplied by the Power Circuit if at least the battery pack is present (+VR after filtering). The P-ASIC indicates the status of the +3V3GAR voltage via the VDDVAL line connected to D-ASIC pin N2. If +3V3GAR is >3V, VDDVAL is high, and the D-ASIC will start-up. As a result the D-ASIC functions are operative regardless of the test tool's is ON/OFF status.
The RAM supply voltage +VR and the FlashROM supply voltage +VF are also derived from +3V3GAR.

Analog to Digital Conversion

For voltage and resistance measurements, the Input A/B (B for voltage only) signal is conditioned by the C-ASIC to 150 mV/division. Zero and gain measurement are done to eliminate offset and gain errors. The C-ASIC output voltage is supplied to the Channel A/B ADC (D401/D451 pin 27). The ADC samples the analog voltage, and converts it into an 8-bit data byte (D0-D7). The data are read and processed by the D-ASIC, see below “ADC data Acquisition”.

The sample rate depends on the sample clock supplied to pin 15. The sample rate is 5 MHz or 25 MHz, depending on the instrument mode. The ADC-A input signal is sampled by sample clock SMPCLK_A; ADC-B by SMPCLK_B. Both sample clocks are generated by the D-ASIC. SMPCLK_B is also used for synchronisation of the Trigger Circuit (B is choosen because of the printed circuit board track layout).

The reference voltages REFADCT and REFADCB determine the input voltage swing that corresponds to an output data swing of 00000000 to 11111111 (D0-D7). The reference voltages are supplied by the reference circuit on the Trigger part. The ADC output voltages MIDADC_A/B are supplied to the C-ASIC’s (input pin 28), and are added to the conditioned input signal. The MIDADC voltage matches the middle of the C-ASIC output swing to the middle of the ADC input swing.

The ADC’s are supplied with +3V3ADCD (supply for digital section; derived from +3V3D) and +3V3ADCA (supply for analog section; derived from +3V3A).

ADC data acquisition for traces and numerical readings

During an acquisition cycle, ADC samples are acquired to complete a trace on the LCD. Numerical readings (METER readings) are derived from the trace. So in single shot mode a new reading becomes available when a new trace is started.

The test tool software starts an acquisition cycle. The D-ASIC acquires data from the ADC, and stores them internally in a cyclic Fast Acquisition Memory (FAM). The D-ASIC also makes the HOLDOFF line low, to enable the T-ASIC to generate the trigger signal TRIGDT. The acquisition cycle is stopped if the required number of samples is acquired. From the FAM the ADC data are moved to the RAM D475. The ADC data stored in the RAM are processed and represented as traces and readings.

Triggering (HOLDOFF, TRIGDT, Randomize)

To start a new trace, the D-ASIC makes the HOLDOFF signal low. Now the T-ASIC can generate the trigger signal TRIGDT. For signal frequencies higher than the system clock frequency, and in the random repetitive sampling mode, no fixed time relation between the HOLDOFF signal and the system clock is allowed. The RANDOMIZE circuit desynchronizes the HOLDOFF from the clock, by phase modulation with a LF ramp signal.

Trigger qualifying (ALLTRIG, TRIGQUAL)

The ALLTRIG signal supplied by the T-ASIC contains all possible triggers. For normal triggering, the T-ASIC uses ALLTRIG to generate the final trigger TRIGDT. For qualified triggering (e.g. TV triggering), the D-ASIC returns a qualified, e.g. each n^{th}, trigger pulse to the T-ASIC (TRIGQUAL). Now the T-ASIC derives the final trigger TRIGDT from the qualified trigger signal TRIGQUAL.

Capacitance measurements (ALLTRIG)

As described in Section 3.3.2, capacitance measurements are based on measuring the capacitor charging time using a known current. The ALLTRIG pulse signal represents the charging time. The time is counted by the D-ASIC

Microprocessor

The D-ASIC includes a microprocessor with a 16 bit data bus. The instrument software is loaded in a 16 Mb Flash ROM D474.

RAM

Measurement data and instrument settings are stored in RAM D475. All RAM data will be lost if all power sources (battery and power adapter) are removed.

mask ROM

The D-ASIC has on-chip mask ROM. If no valid Flash ROM software is present when the test tool is turned on, the mask ROM software will become active. The test tool can be forced to stay in the mask ROM software by keeping pressed the ^ and > keys, and then turning the test tool on. When active, the mask ROM software generates a HF triangular wave on measurement spot MS433 (pin C5 of the D-ASIC).

Controlled switch off

The programmable logic device D470 (CPLD) provides a controlled power down of the D-ASIC. In case of a non-controlled power down, a 6 mA D-ASIC supply current can flow after switching the test tool off. The normal D-ASIC supply current at power off should be below 1 mA (with the mains adapter disconnected).

Watchdog

In case that a software hang-up arises, the watchdog circuit D473 will reset the D-ASIC to re-start the software.

Display Control

The LCD unit includes the LCD, the LCD drivers, and the fluorescent back light lamp. It is connected to the main board via connector X453. The LCD is built up of 240 columns of 240 pixels each (240x240 matrix). The D-ASIC supplies the data and control signals for the LCD drivers on the LCD unit (Figure 3-13).

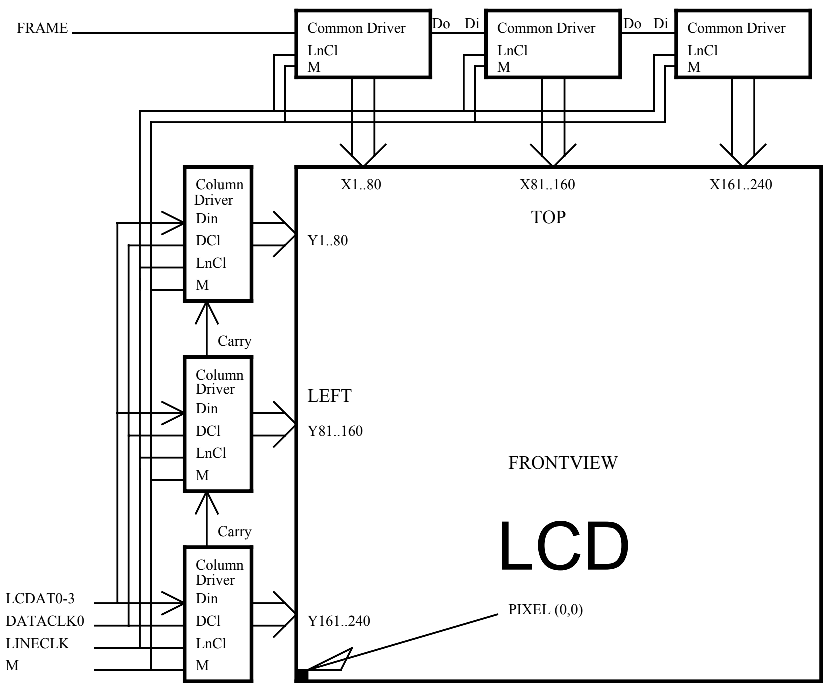


Figure 3-13. LCD Control

Each 14 ms the LCD picture is refreshed during a frame. The frame pulse (FRAME) indicates that the concurrent LINECLK pulse is for the first column. The column drivers must have been filled with data for the first column. Data nibbles (4 bit) are supplied via lines LCDAT0-LCDAT3. During 20 data clock pulses (DATACLK0) the driver for Y161..240 is filled. When it is full, it generates a carry to enable the driver above it, which is filled now. When a column is full, the LINECLK signal transfers the data to the column driver outputs. Via the common drivers, the LINECLK also selects the next column to be filled. So after 240 column clocks a full screen image is built up on the LCD.

The LCD unit generates various voltage levels for the LCD drivers outputs to drive the LCD. The various levels are supplied to the driver outputs, depending on the supplied data and the M(ultiplex) signal. The M signal (back plane modulation) is used by the LCD drivers to supply the various DC voltages in such an order, that the average voltage does not contain a DC component. A DC component in the LCD drive voltage may cause memory effects in the LCD.

The LCD contrast is controlled by the CONTRAST voltage. This voltage is controlled by the D-ASIC, which supplies a PWM signal (pin B12, CONTR-D) to PWM filter R436/C436. The voltage REFPWM1 is used as bias voltage for the contrast adjustment circuit on the LCD unit. To compensate for contrast variations due to temperature variations, a temperature dependent resistor is mounted in the LCD unit. It is connected to the LCDTEMP1 line. The resistance change, which represents the LCD temperature, is measured by the D-ASIC via the S-ADC on the POWER part.
The back light lamp is located at the left side of the LCD, so this side becomes warmer than the right side. As a result the contrast changes from left to right. To eliminate this unwanted effect, the CONTRAST control voltage is increased during building up a screen image. A FRAME pulse starts the new screen image. The FRAME pulse is also used to discharge C404. After the FRAME pulse, the voltage on C404 increases during building up a sreen image.

PWM Signals

The D-ASIC generates various pulse signals, by alternately connecting an output port to a reference voltage (REFPWM1 or REFPWM2) and ground level , with software controllable duty cycle (pins B13-C9). The duty cycle of the pulses is controlled by the software. By filtering the pulses in low pass filters (RC), software controlled DC voltages are generated. The voltages are used for various control purposes, as shown in Table 3-6.

Table 3-6. D-ASIC PWM Signals

PWM signal	Function	Destination	Reference
HO-RNDM	HOLDOFF randomize control	R487 of RANDOMIZE circuit	REFPWM1
TRGLEV1D, TRIGLEV2D	Trigger level control	T-ASIC	REFPWM1
POS-AD, POS-BD	Channel A,B position control	C-ASIC	REFPWM1
OFFSETAD, OFFSETBD	Channel A,B offset control	C-ASIC	REFPWM1
BACKBRIG	Back light brightness control	Back light converter (POWER part)	REFPWM1
CONTR-D	Display contrast control	LCD unit	REFPWM1
SADCLEVD	S ADC comparator voltage	SLOW ADC (POWER part)	REFPWM2
CHARCURD	Battery charge current control	P-ASIC	REFPWM2

Keyboard Control, ON/OFF Control

The keys are arranged in a 6 rows x 6 columns matrix. If a key is pressed, the D-ASIC drives the rows, and senses the columns. The ON/OFF key is not included in the matrix. This key toggles a flip-flop in the D-ASIC via the ONKEY line (D-ASIC pin F4). As the D-ASIC is permanently powered, the flip-flop can signal the test tool on/off status.

SDA-SCL Serial Bus

The unidirectional SDA-SCL serial bus (pin A2, A3) is used to send control data to the C-ASIC's (e.g. change attenuation factor), and the T-ASIC (e.g. select other trigger source). The SDA line transmits the data bursts, the SCL line transmits the synchronization clock (1.25 MHz).

TXD, RXD Serial Interface (Optical Port)

The optical interface output is directly connected to the TXD line (pin L1). The optical input line is buffered by the P-ASIC on the power part. The buffered line is supplied to the RXD input (pin L2). The serial data communication (RS232) is controlled by the D-ASIC.

Slow ADC Control, SADC Bus

The SELMUX0-2 (pins N1, N3, N4) and SLOWADC (pin A4) lines are used for measurements of various analog signals, as described in Section 3.3.1. "SLOW ADC".

BATIDENT

The BATTIDENT/BATIDGAR line (pin B5) is connected to R508 on the Power part, and to a resistor in the battery pack (0 Ω for Ni-Cd, 825 Ω for Ni-MH). If the battery is removed, this is signaled to the D-ASIC (BATTIDENT line goes high).

MAINVAL, FREQPS

The MAINVAL signal (pin M2) is supplied by the P-ASIC, and indicates the presence of the power adapter voltage (high = present).

The FREQPS signal (pin M3) is also supplied by the P-ASIC. It is the same signal that controls the Fly Back Converter control voltage FLYGATE. The D-ASIC measures the frequency in order to detect if the Fly Back Converter is running within specified frequency limits.

D-ASIC Clocks

A 32 kHz oscillator runs if the 3V3GAR supply voltage is present, so if any power source is present (crystal B401). The clock activates the Power On/Off control circuit and the instrument's Real Time Clock (time and date).
A 50 MHz oscillator runs if the test tool is ON, and/or if the power adapter voltage is present (B403).
A 3.6864 MHz UART oscillator for the serial RS232 communication runs if the 50 MHz oscillator runs (B402).

Buzzer

The Buzzer is directly driven by a 4 kHz square wave from the D-ASIC (pin T4) via FET V522. If the test tool is on, the -30VD supply from the Fly Back converter is present, and the buzzer sounds loudly. If the -30VD is not present, the buzzer sounds weak, e.g. when the Mask Active mode is entered.

Chapter 4
Performance Verification

Title	Page

4.1 Introduction

Warning

Procedures in this chapter should be performed by qualified service personnel only. To avoid electrical shock, do not perform any servicing unless you are qualified to do so.

The test tool should be calibrated and in operating condition when you receive it.

The following performance tests are provided to ensure that the test tool is in a proper operating condition. If the test tool fails any of the performance tests, calibration adjustment (see Chapter 5) and/or repair (see Chapter 7) is necessary.

The Performance Verification Procedure is based on the specifications, listed in Chapter 2 of this Service Manual. The values given here are valid for ambient temperatures between 18 °C and 28 °C.

The Performance Verification Procedure is a quick way to check most of the test tool's specifications. Because of the highly integrated design of the test tool, it is not always necessary to check all features separately. For example: the duty cycle, pulse width, and frequency measurement are based on the same measurement principles; so only one of these functions needs to be verified.

4.2 Equipment Required For Verification

The primary source instrument used in the verification procedures is the Fluke 5500A. If a 5500A is not available, you can substitute another calibrator as long as it meets the minimum test requirements.

- Fluke 5500A Multi Product Calibrator, including 5500A-SC Oscilloscope Calibration Option.
- Stackable Test Leads (4x), supplied with the 5500A.
- 50Ω Coax Cables (2x), Fluke PM9091 (1.5m) or PM9092 (0.5m).
- 50Ω feed through terminations (2x), Fluke PM9585.
- Fluke BB120 Shielded Banana to Female BNC adapters (2x), supplied with the Fluke 123.
- Dual Banana Plug to Female BNC Adapter (1x), Fluke PM9081/001.
- Dual Banana Jack to Male BNC Adapter (1x), Fluke PM9082/001.
- TV Signal Generator, Philips PM5418.
- 75Ω Coax cable (1x), Fluke PM9075.
- 75Ω Feed through termination (1x), ITT-Pomona model 4119-75.
- PM9093/001 Male BNC to Dual Female BNC Adapter

4.3 How To Verify

Verification procedures for the display function and measure functions follow. For each procedure the test requirements are listed. If the result of the test does not meet the requirements, the test tool should be recalibrated or repaired if necessary.
Some of the tests are slightly different for Fluke 123 and Fluke 124. This is caused by

the higher vertical and trigger bandwidth in Fluke 124. Differences in requirements for Fluke 123 and Fluke 124 are clearly indicated.

Follow these general instructions for all tests:

- For all tests, power the test tool with the PM8907 power adapter. The battery pack must be installed.
- Allow the 5500A to satisfy its specified warm-up period.
- For each test point , wait for the 5500A to settle.
- Allow the test tool a minimum of 20 minutes to warm up.

4.4 Display and Backlight Test

Proceed as follows to test the display and the backlight:

1. Press to turn the Test tool on.
2. Fluke 123: press and verify that the backlight is dimmed. Then select maximum backlight brightness again.
   Fluke 124: press , then press F3 . Verify that the test tool can be switched between dimmed backlight and maximum brightness with the keys. During the tests, use maximum brightness for the best visibility.
3. Remove the adapter power, and verify that the backlight is dimmed.
4. Apply the adapter power and verify that the backlight brightness is set to maximum.
5. Press and hold .
6. Press and release F4.
7. Release .
   The test tool shows the calibration menu in the bottom of the display.

   Do not press F3 now! If you did, turn the test tool off and on, and start at 5.
8. Press F1 (PREV) three times.
   The test tool shows **Contrast (CL 0100):MANUAL**
9. Press F3 (CAL) .
   The test tool shows a dark display; the test pattern as shown in Figure 4-1 may not be visible or hardly visible.
   Observe the display closely, and verify that no light pixels are shown.

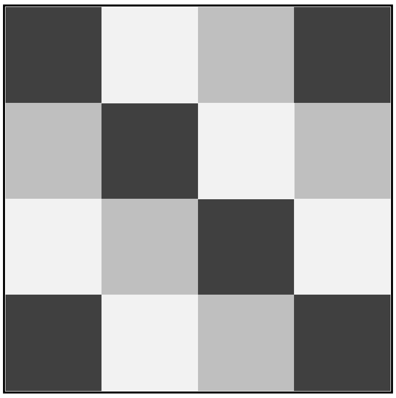


Figure 4-1. Display Pixel Test Pattern

11. Press F2.
    The test pattern is removed; the test tool shows **Contrast (CL 0110):MANUAL**
12. Press F3 (CAL) .
    The test tool shows the display test pattern shown in Figure 4-1, at default contrast. Observe the test pattern closely, and verify that the no pixels with abnormal contrast are present in the display pattern squares. Also verify that the contrast of the upper left and upper right square of the test pattern are equal.
13. Press F2.
    The test pattern is removed; the test tool shows **Contrast (CL 0120):MANUAL**
14. Press F3 (CAL) .
    The test tool shows a light display; the test pattern as shown in Figure 4-1 may not be visible or hardly visible.
    Observe the display closely, and verify that no dark pixels are shown.
15. Turn the test tool OFF and ON to exit the calibration menu and to return to the normal operating mode.

4.5 Input A and Input B Tests

Before performing the Input A and Input B tests, the test tool must be set in a defined state, by performing a RESET.

Proceed as follows to reset the test tool:

- Press to turn the test tool off.
- Press and hold .
- Press and release to turn the test tool on.

Wait until the test tool has **beeped twice**, and then release . When the test tool has beeped twice, the RESET was successful.

For most tests, you must turn Input B on. Input A is always on.

Proceed as follows to turn Input B on:

- Press VHzA to open the Meter B menu.

- Using select **INPUT B: ON** .
- Press to confirm the selection; the mark changes to ■ . The active setting from the next item group will be highlighted (for example ■ **VAC**), and maintained after leaving the menu.
- Press to exit the menu.

During verification you must open menus, and to choose items from the menu.

Proceed as follows to make choices in a menu (see Figure 4.2):

- Open the menu, for example press SCOPE MENU .
- Press to highlight the item to be selected in a menu.
- Press F4 to confirm the selection and to jump to the next item group (if present). Item groups in a menu are separated by a vertical line.
- After pressing F4 in the last menu item group, the menu is closed.

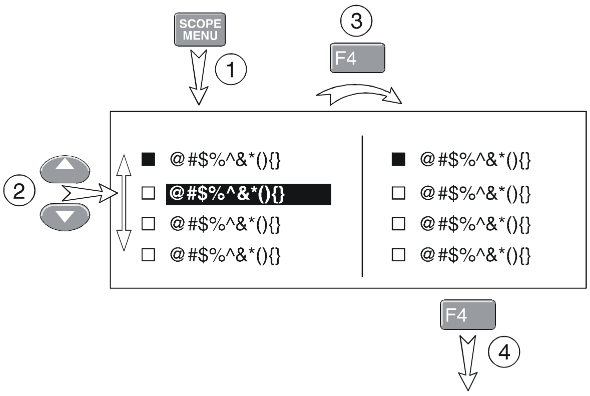


Figure 4-2. Menu item selection

If an item is selected, it is marked by ■. Not selected items are marked by . If a selected item is highlighted, an then F4 is pressed, the item remains selected.

You can also navigate through the menu using . To conform the highlighted item you must press F4.

4.5.1 Input A and B Base Line Jump Test

Proceed as follows to check the Input A and Input B base line jump:

1. Short circuit the Input A and the Input B shielded banana sockets of the test tool. Use the BB120 banana to BNC adapter, and a 50Ω (or lower) BNC termination.
2. Select the following test tool setup:
   - Turn Input B on (if not already on).
   - Press AUTO to select auto ranging (**AUTO** in top of display). (AUTO toggles between **AUTO** and **MANUAL** ranging).
   - Press SCOPE MENU to open the SCOPE INPUTS menu.
   - Press F1 to open the SCOPE OPTIONS menu, and choose :

SCOPE MODE: ■ NORMAL | WAVEFORM MODE: ■ SMOOTH

3. Using s TIME ns toggle the time base between 10 ms/div and 5 ms/div.
   (the time base ranging is set to manual now, the input sensitivity is still automatic; no indication **AUTO** or **MANUAL** is displayed).
   After changing the time base wait some seconds until the trace has settled.

   Observe the Input A trace, and check to see if it returns to the same position after changing the time base. The allowed difference is ±0.04 division (= 1 pixel).

   Observe the Input B trace for the same conditions.

4. Using s TIME ns toggle the time base between 1 µs/div and 500 ns/div. After changing the time base wait some seconds until the trace has settled.

   Observe the Input A trace, and check to see if it is set to the same position after changing the time base. The allowed difference is ±0.04 division (= 1 pixel).

   Observe the Input B trace for the same conditions.

5. Using s TIME ns set the time base to 10 ms/div.

6. Using mV V toggle the sensitivity of Input A between 5 and 10 mV/div. After changing the sensitivity wait some seconds until the trace has settled.

   Observe the Input A trace, and check to see if it is set to the same position after changing the sensitivity. The allowed difference is ±0.04 division (= 1 pixel).

7. Using mV V toggle the sensitivity of Input B between 5 and 10 mV/div. After changing the sensitivity wait some seconds until the trace has settled.

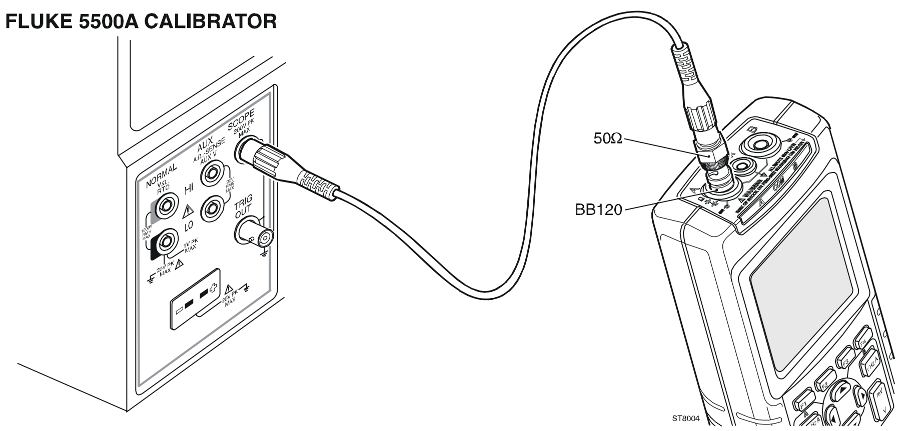
   Observe the Input B trace, and check to see if it is set to the same position after changing the sensitivity. The allowed difference is ±0.04 division (= 1 pixel).

8. When you are finished, remove the Input A and Input B short.

4.5.2 Input A Trigger Sensitivity Test

Proceed as follows to test the Input A trigger sensitivity:

1. Connect the test tool to the 5500A as shown in Figure 4-3.



ST8004.WMF

Figure 4-3. Test Tool Input A to 5500A Scope Output 50Ω

2. Select the following test tool setup:

- Press AUTO to select auto ranging (**AUTO** in top of display).
  Do not press s TIME ns anymore!
- Using mV V change the sensitivity to select manual sensitivity ranging, and lock the Input A sensitivity on 200 mV/div.

3. Set the 5500A to source a 5 MHz leveled sine wave of 100 mV peak-to-peak (SCOPE output, MODE levsin).
4. Adjust the amplitude of the sine wave to 0.5 division on the display.
5. Verify that the signal is well triggered.
   If it is not, press F3 to enable the up/down arrow keys for Trigger Level adjustment; adjust the trigger level using ▲▼ and verify that the signal will be triggered now. The trigger level is indicated by the trigger icon (⌠).
6. Set the 5500A to source a 25 MHz (Fluke 123) or 40 MHz (Fluke 124) leveled sine wave of 400 mV peak-to-peak.
7. Adjust the amplitude of the sine wave to 1.5 divisions on the test tool display.
8. Verify that the signal is well triggered.
   If it is not, press F3 to enable the up/down arrow keys for Trigger Level adjustment; adjust the trigger level and verify that the signal will be triggered now.
9. Set the 5500A to source a 40 MHz (Fluke 123) or 60 MHz (Fluke 124) leveled sine wave of 1.8V peak-to-peak.
10. Adjust the amplitude of the sine wave to 4 divisions on the test tool display.
11. Verify that the signal is well triggered.
    If it is not, press F3 to enable the up/down arrow keys for Trigger Level adjustment; adjust the trigger level and verify that the signal will be triggered now.
12. When you are finished, set the 5500A to Standby.

4.5.3 Input A Frequency Response Upper Transition Point Test

Proceed as follows to test the Input A frequency response upper transition point:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-3).
2. Select the following test tool setup:
   - Press AUTO to select auto ranging (**AUTO** in top of display).
     Do not press s TIME ns anymore!
   - Using mV V change the sensitivity to select manual sensitivity ranging, and lock the Input A sensitivity on 200 mV/div.
3. Set the 5500A to source a leveled sine wave of 1.2V peak-to-peak, 50 kHz (SCOPE output, MODE levsin).
4. Adjust the amplitude of the sine wave to 6 divisions on the test tool display.
5. Set the 5500A to 20 MHz (Fluke 123) or 40 MHz (Fluke 124), without changing the amplitude.
6. Observe the Input A trace check to see if it is ≥ 4.2 divisions.
7. When you are finished, set the 5500A to Standby.

Note
The lower transition point is tested in Section 4.5.11.

4.5.4 Input A Frequency Measurement Accuracy Test

Proceed as follows to test the Input A frequency measurement accuracy:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-3).
2. Select the following test tool setup:
   - Press AUTO to select auto ranging (**AUTO** in top of display).
   - Press VHzA Ω to open the INPUT A MEASUREMENTS menu, and choose:

     MEASURE on A: ■ Hz
3. Set the 5500A to source a leveled sine wave of 600 mV peak-to-peak (SCOPE output, MODE levsin).
4. Set the 5500A frequency according to the first test point in Table 4-1.
5. Observe the Input A main reading on the test tool and check to see if it is within the range shown under the appropriate column.
6. Continue through the test points.
7. When you are finished, set the 5500A to Standby.

Table 4-1. Input A,B Frequency Measurement Accuracy Test

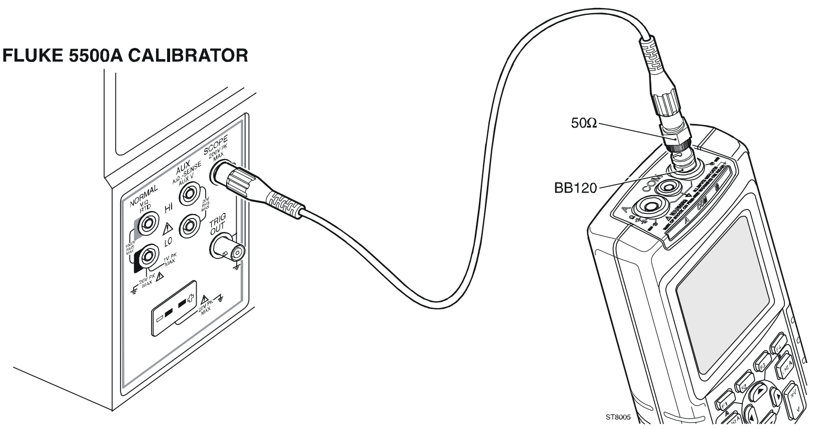
5500A output, 600 mVpp	Input A, B Reading
1 MHz	0.993 to 1.007 MHz
10 MHz	09.88 to 10.12 MHz
40 MHz	38.98 to 41.02 MHz
60 MHz (Fluke 124 only)	58.48 to 61.52 MHz

Note
Duty Cycle and Pulse Width measurements are based on the same principles as Frequency measurements. Therefore the Duty Cycle and Pulse Width measurement function will not be verified separately.

4.5.5 Input B Frequency Measurement Accuracy Test

Proceed as follows to test the Input B frequency measurement accuracy:

1. Connect the test tool to the 5500A as shown in Figure 4-4.



ST8005.WMF

Figure 4-4. Test Tool Input B to 5500A Scope Output 50Ω

2. Select the following test tool setup:
   - Press AUTO select auto ranging (**AUTO** in top of display).
   - Press VHzA to open the INPUT B MEASUREMENTS menu, and choose:

     INPUT B: ■ ON | MEASURE on B: ■ Hz
   - Press SCOPE MENU to open the SCOPE INPUTS menu.
   - Press F3 to open the TRIGGER menu, and choose:

     INPUT: ■ B | SCREEN UPDATE: ■ FREE RUN | AUTO RANGE: ■ >15HZ
3. Set the 5500A to source a leveled sine wave of 600 mV peak-to-peak (SCOPE output, MODE levsin).
4. Set the 5500A frequency according to the first test point in Table 4-1.
5. Observe the Input B main reading on the test tool and check to see if it is within the range shown under the appropriate column.
6. Continue through the test points.
7. When you are finished, set the 5500A to Standby.

4.5.6 Input B Frequency Response Upper Transition Point Test

Proceed as follows to test the Input B frequency response upper transition point:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-4).
2. Select the following test tool setup:
   - Turn Input B on (if not already on).
   - Press AUTO to select auto ranging (**AUTO** in top of display).
     Do not press s TIME ns anymore!
   - Using mV V change the sensitivity to select manual sensitivity ranging, and lock the Input B sensitivity on 200 mV/div.
   - Press SCOPE MENU to open the SCOPE INPUTS menu.
   - Press F3 to open the TRIGGER menu, and choose:

INPUT: ■ B | SCREEN UPDATE: ■ FREE RUN | AUTO RANGE: ■ >15HZ

3. Set the 5500A to source a leveled sine wave of 1.2V peak-to-peak, 50 kHz (SCOPE output, MODE levsin).
4. Adjust the amplitude of the sine wave to 6 divisions on the test tool display.
5. Set the 5500A to 20 MHz (Fluke 123) or 40 MHz (Fluke 124), without changing the amplitude.
6. Observe the Input B trace check to see if it is ≥ 4.2 divisions.
7. When you are finished, set the 5500A to Standby.

Note

The lower transition point is tested in Section 4.5.11.

4.5.7 Input B Trigger Sensitivity Test

Proceed as follows to test the Input B trigger sensitivity:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-4).
2. Select the following test tool setup:
   - Turn Input B on (if not already on).
   - Press AUTO to select auto ranging (**AUTO** in top of display).
     Do not press s TIME ns anymore!
   - Using mV V change the sensitivity to select manual sensitivity ranging, and lock the Input B sensitivity on 200 mV/div.
   - Press SCOPE MENU to open the SCOPE INPUTS menu.
   - Press F3 to open the TRIGGER menu, and choose:

   INPUT: ■ B | SCREEN UPDATE: ■ FREE RUN | AUTO RANGE: ■ >15HZ
3. Set the 5500A to source a 5 MHz leveled sine wave of 100 mV peak-to-peak (SCOPE output, MODE levsin).
4. Adjust the amplitude of the sine wave to 0.5 division on the display.
5. Verify that the signal is well triggered.
   If it is not, press F3 to enable the up/down arrow keys for Trigger Level adjustment; adjust the trigger level and verify that the signal will be triggered now.
   The trigger level is indicated by the trigger icon (⅃).
6. Set the 5500A to source a 25 MHz (Fluke 123) or 40 MHz (Fluke 124) leveled sine wave of 400 mV peak-to-peak.
7. Adjust the amplitude of the sine wave 1.5 divisions on the test tool display.
8. Verify that the signal is well triggered.
   If it is not, press F3 to enable the up/down arrow keys for Trigger Level adjustment; adjust the trigger level and verify that the signal will be triggered now.
9. Set the 5500A to source a 40 MHz (Fluke 123) or 60 MHz (Fluke 124) leveled sine wave of 1.8V peak-to-peak.
10. Adjust the amplitude of the sine wave to exactly 4 divisions on the test tool display.

11. Verify that the signal is well triggered.
    If it is not, press F3 to enable the up/down arrow keys for Trigger Level adjustment; adjust the trigger level and verify that the signal will be triggered now.
12. When you are finished, set the 5500A to Standby.

4.5.8 Input A and B Trigger Level and Trigger Slope Test

Proceed as follows:

1. Connect the test tool to the 5500A as shown in Figure 4-5.

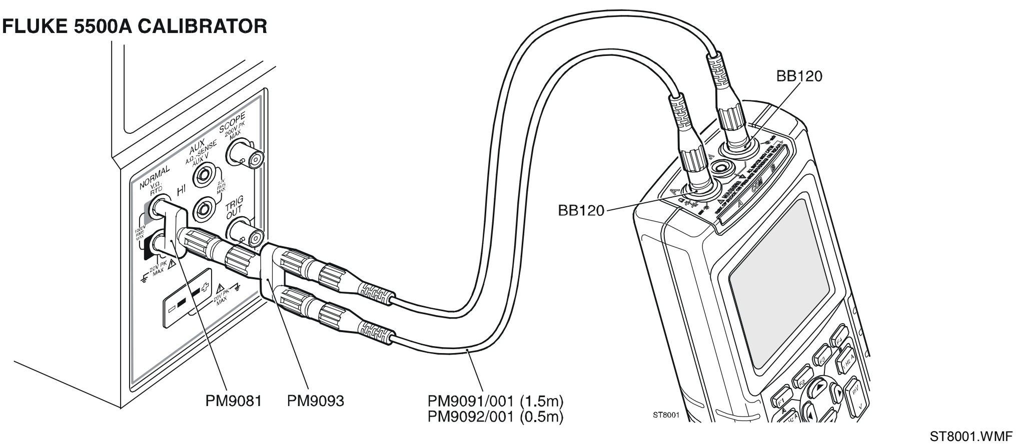


Figure 4-5. Test Tool Input A-B to 5500A Normal Output

2. Select the following test tool setup:
   - Turn Input B on (if not already on).
   - Using mV V change the sensitivity to select manual sensitivity ranging, and lock the Input A and Input B sensitivity on 1V/div.
   - Move the Input A and Input B ground level (indicated by zero icon ■) to the center grid line. Proceed as follows:

     Press F1 to enable the arrow keys for moving the Input A ground level.

     Press F2 to enable the arrow keys for moving the Input B ground level.

     Using the ▲▼ keys move the ground level.
   - Using s TIME ns change the time base to select manual time base ranging, and lock the time base on 10 ms/div.
   - Press SCOPE MENU to open the SCOPE INPUTS menu.
   - Press F3 to open the TRIGGER menu, and choose:

     INPUT: ■ A | SCREEN UPDATE: ■ FREE RUN | AUTO RANGE: ■ >15HZ
   - Press F3 to enable the arrow keys for Trigger Level and Slope adjustment.
   - Using ◄► select positive slope triggering (trigger icon ⌐).
   - Using ▲▼ set the trigger level to +2 divisions from the screen center. For **positive slope** triggering, the trigger level is the **top** of the trigger icon (⌐).

- Press SCOPE MENU to open the SCOPE INPUTS menu.
- Press F1 to open the SCOPE OPTIONS menu, and choose:

  SCOPE MODE: ■ SINGLE SHOT | WAVEFORM MODE: ■ NORMAL

3. Set the 5500A to source 0.4V DC.
4. Verify that no trace is shown on the test tool display, and that the status line at the display bottom shows **Wait:A ⎍**. If the display shows the traces and status **Hold:A ⎍**, then press HOLD RUN to re-arm the test tool for a trigger.
5. Increase the 5500A voltage slowly in 0.1V steps, using the 5500A EDIT FIELD function, until the test tool is triggered, and the traces are shown.
6. Verify that the 5500A voltage is between **+1.5V and +2.5V** when the test tool is triggered. To repeat the test, start at step 3.
7. Set the 5500A to Standby.
8. Press HOLD RUN to clear the display.
9. Press F3 to enable the arrow keys for Trigger Level and Slope adjustment.
10. Using ◀▶ select negative slope triggering (⎍).
11. Using ▲▼ set the trigger level to +2 divisions from the screen center. For **negative slope** triggering, the trigger level is the **bottom** of the trigger icon (⎍).
12. Set the 5500A to source +3V DC.
13. Verify that no trace is shown on the test tool display, and that the status line at the display bottom shows **Wait:A⎍**. If the display shows the traces and status **Hold:A⎍**, then press HOLD RUN to re-arm the test tool for a trigger.
14. Decrease the 5500A voltage slowly in 0.1V steps, using the 5500A EDIT FIELD function, until the test tool is triggered, and the traces are shown.
15. Verify that the 5500A voltage is between **+1.5V and +2.5V** when the test tool is triggered. To repeat the test, start at step 12.
16. Set the 5500A to Standby.
17. Press HOLD RUN to clear the display.
18. Select the following test tool setup:
    - Press SCOPE MENU to open the SCOPE INPUTS menu.
    - Press F3 to open the TRIGGER menu, and choose:

      INPUT: ■ B | SCREEN UPDATE: ■ FREE RUN | AUTO RANGE: ■ >15HZ

    - Press F3 to enable the arrow keys for Trigger Level and Slope adjustment.
    - Using ◀▶ select positive slope triggering (trigger icon ⎍).
    - Using ▲▼ set the trigger level to +2 divisions from the screen center. For **positive slope** triggering, the trigger level is the **top** of the trigger icon (⎍).
19. Set the 5500A to source 0.4V DC.

20. Verify that no trace is shown on the test tool display, and that the status line at the display bottom shows **Wait:B** ⨍. If the display shows the traces and status **Hold:B** ⨍, then press HOLD RUN to re-arm the test tool for a trigger.
21. Increase the 5500A voltage slowly in 0.1V steps, using the 5500A EDIT FIELD function, until the test tool is triggered, and the traces are shown.
22. Verify that the 5500A voltage is between **+1.5V and +2.5V** when the test tool is triggered.
    To repeat the test, start at step 19.
23. Set the 5500A to Standby.
24. Press HOLD RUN to clear the display.
25. Press F3 to enable the arrow keys for Trigger Level and Slope adjustment.
26. Using ◀▶ select negative slope triggering (⨏).
27. Using ▲▼ set the trigger level to +2 divisions from the screen center. For **negative slope** triggering, the trigger level is the **bottom** of the trigger icon (⨏).
28. Set the 5500A to source +3V DC.
29. Verify that no trace is shown on the test tool display, and that the status line at the display bottom shows **Wait:B**⨏. If the display shows the traces and status **Hold:B**⨏, then press HOLD RUN to re-arm the test tool for a trigger.
30. Decrease the 5500A voltage in 0.1V steps, using the 5500A EDIT FIELD function, until the test tool is triggered, and the traces are shown.
31. Verify that the 5500A voltage is between **+1.5V and +2.5V** when the test tool is triggered. To repeat the test, start at step 28.
32. When you are finished, set the 5500A to Standby.

4.5.9 Input A and B DC Voltage Accuracy Test

WARNING

Dangerous voltages will be present on the calibration source and connecting cables during the following steps. Ensure that the calibrator is in standby mode before making any connection between the calibrator and the test tool.

Proceed as follows:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-5).
2. Select the following test tool setup:
    - Press AUTO select auto ranging (**AUTO** in top of display).
    - Press VHzA Ω to open the INPUT A MEASUREMENTS menu, and choose:

      MEASURE on A: ■ VDC
    - Press VHzA to open the INPUT B MEASUREMENTS menu, and choose:

      INPUT B: ■ ON | MEASURE on B: ■ VDC

- Using [s TIME ns] change the time base to select manual time base ranging, and lock the time base on 10 ms/div.
- Press [SCOPE MENU] to open the SCOPE INPUTS menu.
- Press [F1] to open the SCOPE OPTIONS menu, and choose:

  SCOPE MODE: ■ NORMAL | WAVEFORM MODE: ■ SMOOTH

- Move the Input A and Input B ground level (indicated by zero icon ■) to the center grid line. Proceed as follows:

  Press [F1] to enable the arrow keys for moving the Input A ground level.

  Press [F2] to enable the arrow keys for moving the Input B ground level.

  Using the [▲][▼] keys move the ground level.

3. Using [mV] [V] set the Input A and B sensitivity to the first test point in Table 4-2. The corresponding range is shown in the second column of the table.
4. Set the 5500A to source the appropriate DC voltage.
5. Observe the main reading and check to see if it is within the range shown under the appropriate column.
6. Continue through the test points.
7. When you are finished, set the 5500A to 0 (zero) Volt, and to Standby.

Table 4-2. Volts DC Measurement Verification Points

Sensitivity (Oscilloscope)	Range 1) (Meter)	5500A output, V DC	Input A-B DC Reading
5 mV/div	500 mV	15 mV	014.4 to 015.6 2)
10 mV/div	500 mV	30 mV	029.3 to 030.7 2)
20 mV/div	500 mV	60 mV	059.2 to 060.8
50 mV/div	500 mV	150 mV	148.7 to 151.3
100 mV/div	500 mV	300 mV	298.0 to 302.0
200 mV/div	500 mV	500 mV	497.0 to 503.0
		-500 mV	-497.0 to -503.0
		0 mV	-000.5 to + 000.5
500 mV/div	5V	1.5V	1.487 to 1.513
1 V/div	5V	3V	2.980 to 3.020
2 V/div	5V	5V	4.970 to 5.030
		-5V	-4.970 to -5.030
		0V	-0.005 to +0.005
5 V/div	50V	15V	14.87 to 15.13
10 V/div	50V	30V	29.80 to 30.20
20 V/div	50V	50V	49.70 to 50.30
		-50V	-49.70 to -50.30
		0V	-00.05 to +00.05
50 V/div	500V	150V	148.7 to 151.3
100 V/div	500V	300V	298.0 to 302.0

1) The 500V and 1250V range will be tested in Section 4.5.14

2) Due to calibrator noise, occasionally OL (overload) can be shown.

4.5.10 Input A and B AC Voltage Accuracy Test

Warning

Dangerous voltages will be present on the calibration source and connecting cables during the following steps. Ensure that the calibrator is in standby mode before making any connection between the calibrator and the test tool.

Proceed as follows to test the Input A and B AC Voltage accuracy:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-5).

2. Select the following test tool setup:

- Press AUTO to select auto ranging (**AUTO** in top of display).
  Do not press s TIME ns anymore!
- Press VHzA Ω to open the INPUT A MEASUREMENTS menu, and choose:

  MEASURE on A: ■ VAC
- Press VHzA to open the INPUT B MEASUREMENTS menu, and choose:

  INPUT B: ■ ON | MEASURE on B: ■ VAC
- Move the Input A and Input B ground level (indicated by zero icon ■) to the center grid line. Proceed as follows:

  Press F1 to enable the arrow keys for moving the Input A ground level.

  Press F2 to enable the arrow keys for moving the Input B ground level.

  Using the ▲▼ keys move the ground level.

3. Using mV V set the Input A and B sensitivity to the first test point in Table 4-3. The corresponding range is shown in the second column of the table.
4. Set the 5500A to source the required AC voltage (NORMAL output, WAVE sine).
5. Observe the Input A and Input B main reading and check to see if it is within the range shown under the appropriate column.
6. Continue through the test points.
7. When you are finished, set the 5500A to Standby.

Table 4-3. Volts AC Measurement Verification Points

Sensitivity (Oscilloscope)	Range [1)] (Meter)	5500A output Volts rms	5500A Frequency	Reading A-B
200 mV/div	500 mV	500 mV	60 Hz	494.0 to 506.0
		500 mV	20 kHz	486.0 to 514.0
2V/div	5V	5V	20 kHz	4.860 to 5.140
		5V	60 Hz	4.940 to 5.060
20V/div	50V	50V	60 Hz	49.40 to 50.60
		50V	20 kHz	48.60 to 51.40

[1)] The 500V and 1250V range will be tested in Section 4.5.14

4.5.11 Input A and B AC Input Coupling Test

Proceed as follows to test the Input A and B AC coupled input lower transition point:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-5).
2. Select the following test tool setup:

- Use the setup of the previous step (AUTO time base, traces at vertical center).
- Using mV V select 200 mV/div for Input A and B (500 mV range).

- Press SCOPE MENU to open the SCOPE INPUTS menu, and choose:

  INPUT A: ■ AC | ■ NORMAL | INPUT B: ■ AC | NORMAL■

- Press SCOPE MENU to open the SCOPE INPUTS menu.
- Press F3 to open the TRIGGER menu, and choose:

  INPUT: A | SCREEN UPDATE: ■ FREE RUN | AUTO RANGE: ■ > 1HZ

3. Set the 5500A to source an AC voltage, to the first test point in Table 4-4 (NORMAL output, WAVE sine).
4. Observe the Input A and Input B main reading and check to see if it is within the range shown under the appropriate column.
5. Continue through the test points.
6. When you are finished, set the 5500A to Standby.

Table 4-4. Input A and B AC Input Coupling Verification Points

5500A output, V rms	5500A Frequency	Reading A-B
500.0 mV	10 Hz	> 344.0
500.0 mV	33 Hz	> 469.0
500.0 mV	60 Hz	> 486.5

4.5.12 Input A and B Volts Peak Measurements Test

WARNING

Dangerous voltages will be present on the calibration source and connecting cables during the following steps. Ensure that the calibrator is in standby mode before making any connection between the calibrator and the test tool.

Proceed as follows to test the Volts Peak measurement function:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-5).
2. Select the following test tool setup:

- Press SCOPE MENU to open the SCOPE INPUTS menu.
- Press F3 to open the TRIGGER menu, and choose:

  INPUT: A | SCREEN UPDATE: ■ FREE RUN | AUTO RANGE: ■ > 15HZ

- Press AUTO to select auto ranging (**AUTO** in top of display).
- Press VHzA Ω to open the INPUT A MEASUREMENTS menu, and choose:

  MEASURE on A: ■ PEAK

  From the INPUT A PEAK sub-menu choose:

  PEAK TYPE : ■ PEAK-PEAK

- Press VHzA to open the INPUT B MEASUREMENTS menu, and choose:

  INPUT B: ■ ON | MEASURE on B: ■ PEAK

From the INPUT B PEAK sub-menu choose:

PEAK TYPE : ■ PEAK-PEAK

- Using [mV] [V] select 1V/div for input A and B.

3. Set the 5500A to source a sine wave, to the first test point in Table 4-5 (NORMAL output, WAVE sine).
4. Observe the Input A and Input B main reading and check to see if it is within the range shown under the appropriate column.
5. Continue through the test points.
6. When you are finished, set the 5500A to Standby.

Table 4-5. Volts Peak Measurement Verification Points

5500A output, Vrms (sine)	5500A Frequency	Reading A-B
1.768 (5V peak)	1 kHz	4.50 to 5.50

4.5.13 Input A and B Phase Measurements Test

Proceed as follows:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-5).
2. Select the following test tool setup:

- Press [AUTO] to select auto ranging (**AUTO** in top of display).
- Press [VHzA Ω] to open the INPUT A MEASUREMENTS menu, and choose:

MEASURE on A: ■ PHASE

- Press [VHzA] to open the INPUT B MEASUREMENTS menu, and choose:

INPUT B: ■ ON | MEASURE on B: ■ PHASE

- Using [mV] [V] select 1V/div for input A and B.

3. Set the 5500A to source a sine wave, to the first test point in Table 4-6 (NORMAL output, WAVE sine).
4. Observe the Input A and Input B main reading and check to see if it is within the range shown under the appropriate column.
5. Continue through the test points.
6. When you are finished, set the 5500A to Standby.

Table 4-6. Phase Measurement Verification Points

5500A output, Vrms (sine)	5500A Frequency	Reading A-B
1.5V	1 kHz	-2 to +2 Deg

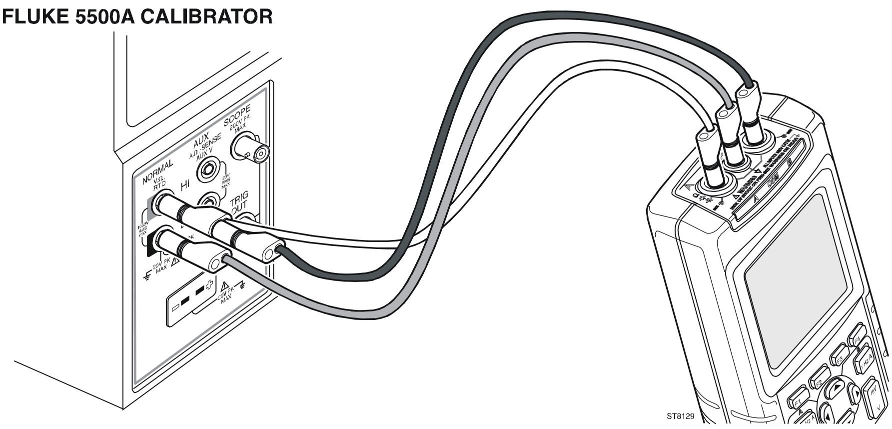
4.5.14 Input A and B High Voltage AC/DC Accuracy Test

Warning

Dangerous voltages will be present on the calibration source and connecting cables during the following steps. Ensure that the calibrator is in standby mode before making any connection between the calibrator and the test tool.

Proceed as follows to test the Input A&B High Voltage AC and DC Accuracy:

1. Connect the test tool to the 5500A as shown in Figure 4-6.



ST8129.WMF

Figure 4-6. Test Tool Input A-B to 5500A Normal Output for >300V

2. Select the following test tool setup:

- Press [AUTO] to select auto ranging (**AUTO** in top of display).
  Do not press [s TIME ns] anymore!
- Press [VHzA Ω] to open the INPUT A MEASUREMENTS menu, and choose:

  MEASURE on A: ■ VAC
- Press [VHzA Ω] to open the INPUT A MEASUREMENTS menu, and choose:

  MEASURE on A: ■ VDC (VDC becomes main reading, VAC secondary reading)
- Press [VHzA] to open the INPUT B MEASUREMENTS menu, and choose:

  INPUT B: ■ ON | MEASURE on B: ■ VAC
- Press [VHzA] to open the INPUT B MEASUREMENTS menu, and choose:

  INPUT B: ■ ON | MEASURE on B: ■ VDC
- Move the Input A and Input B ground level (indicated by zero icon ■) to the center grid line. Proceed as follows:

  Press [F1] to enable the arrow keys for moving the Input A ground level.

  Press [F2] to enable the arrow keys for moving the Input B ground level.

  Using the [▲][▼] keys move the ground level.

3. Using mV V set the Input A and B sensitivity to the first test point in Table 4-7. The corresponding range is shown in the second column of the table.
4. Set the 5500A to source the required AC voltage (NORMAL output, WAVE sine).
5. Observe the Input A and B main reading (V DC) and secondary reading (V-AC) and check to see if it is within the range shown under the appropriate column.
6. Continue through the test points.
7. When you are finished, set the 5500A to Standby

Table 4-7. V DC and V AC High Voltage Verification Tests

Sensitivity (Scope)	Range (Meter)	5500A output Vrms	5500A Frequency	Main (DC) Reading A-B	Secondary (AC) Reading A-B
200V/div	500V	0V	DC	-000.5 to +000.5	
		+500V	DC	+497.0 to +503.0	
		-500V	DC	-497.0 to -503.0	
		500V	60Hz		494.0 to 506.0
		500V	10 kHz		486.0 to 514.0
500V/div	1250V	600V	10 kHz		0.570 to 0.630
		600V	60Hz		0.584 to 0.616
		+600V	DC	+0.592 to +0.608	
		-600V	DC	-0.592 to -0.608	
		0V	DC	-0.005 to +0.005	

4.5.15 Resistance Measurements Test

Proceed as follows:

1. Connect the test tool to the 5500A as shown in Figure 4-7.

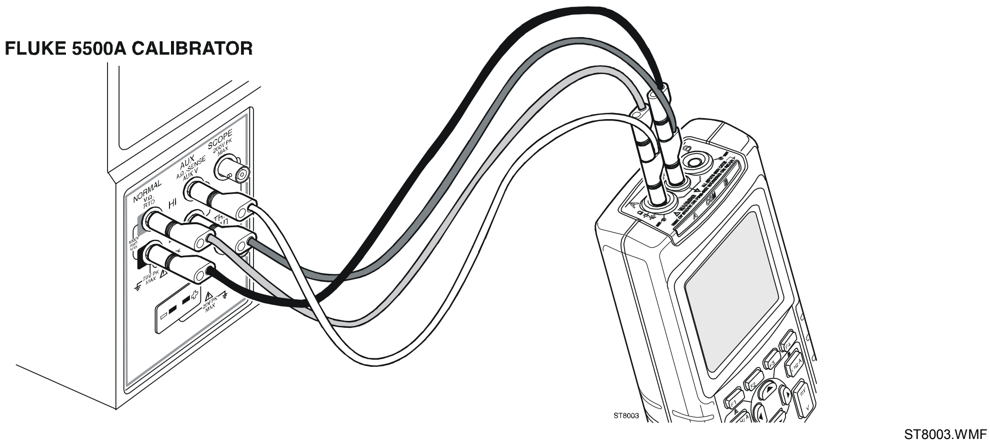


Figure 4-7. Test Tool Input A to 5500A Normal Output 4-Wire

2. Select the following test tool setup:
   - Press AUTO to select auto ranging (**AUTO** in top of display).
   - Press VHzA Ω to open the INPUT A MEASUREMENTS menu, and choose:

     MEASURE on A: ■ OHM Ω
3. Set the 5500A to the first test point in Table 4-8.
   Use the 5500A “COMP 2 wire” mode for the verifications up to and including 50 kΩ. For the higher values, the 5500A will turn off the “COMP 2 wire” mode.
4. Observe the Input A main reading and check to see if it is within the range shown under the appropriate column.
5. Continue through the test points.
6. When you are finished, set the 5500A to Standby.

Table 4-8. Resistance Measurement Verification Points

5500A output	Reading
0Ω	000.0 to 000.5
400Ω	397.1 to 402.9
4 kΩ	3.971 to 4.029
40 kΩ	39.71 to 40.29
400 kΩ	397.1 to 402.9
4 MΩ	3.971 to 4.029
30 MΩ	29.77 to 30.23

4.5.16 Continuity Function Test

Proceed as follows:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-7).
2. Select the following test tool setup:
   - Press AUTO to select auto ranging (**AUTO** in top of display).
   - Press VHzA Ω to open the INPUT A MEASUREMENTS menu, and choose:

     MEASURE on A: ■ CONT)))
3. Set the 5500A to 25Ω. Use the 5500A “COMP 2 wire” mode.
4. Listen to hear that the beeper sounds continuously.
5. Set the 5500A to 35Ω.
6. Listen to hear that the beeper does not sound.
7. When you are finished, set the 5500A to Standby.

4.5.17 Diode Test Function Test

Proceed as follows to test the Diode Test function :

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-7).
2. Press VHzA Ω to open the INPUT A MEASUREMENTS menu, and choose:

   MEASURE on A: ■ DIODE
3. Set the 5500A to **1 kΩ**. Use the 5500A “COMP 2 wire” mode.
4. Observe the main reading and check to see if it is within 0.425 and 0.575V.
5. Set the 5500A to **1V DC.**
6. Observe the main reading and check to see if it is within 0.975 and 1.025V.
7. When you are finished, set the 5500A to Standby.

4.5.18 Capacitance Measurements Test

Proceed as follows:

1. Connect the test tool to the 5500A as for the previous test (see Figure 4-7). Ensure that the 5500A is in Standby.
2. Select the following test tool setup:
   - Press VHzA Ω to open the INPUT A MEASUREMENTS menu, and choose:

     MEASURE on A: ■ CAP
   - Press AUTO to select auto ranging (**AUTO** in top of display).
   - Press VHzA Ω to open the INPUT A MEASUREMENTS menu.
   - Press F1 the select the METER A OPTIONS MENU, and choose:

     SMOOTHING: ■ NORMAL | ZERO REF: ■ ON

   The ZERO REF function is used to eliminate the capacitance of the test leads.
3. Set the 5500A to the first test point in Table 4-9. Use the 5500A “COMP OFF” mode.
4. Observe the Input A main reading and check to see if it is within the range shown under the appropriate column.
5. Continue through the test points.
6. When you are finished, set the 5500A to Standby.
7. Remove all test leads from the test tool to check the zero point.
8. Press VHzA Ω to open the INPUT A MEASUREMENTS menu.
9. Press F1 the select the METER A OPTIONS MENU, and choose:

   SMOOTHING: ■ NORMAL | ZERO REF: ■ OFF
10. Observe the Input A reading and check to see if it is between 00.00 and 00.10 nF.

Table 4-9. Capacitance Measurement Verification Points

5500A output	Reading
40 nF	39.10 to 40.90
300 nF	293.0 to 307.0
3 μF	2.930 to 3.070
30 μF	29.30 to 30.70
300 μF	293.0 to 307.0
0 (remove test tool input connections)	00.00 to 00.10 (see steps 7...10)

4.5.19 Video Trigger Test

Only one of the systems NTSC, PAL, or SECAM has to be verified.

Proceed as follows:

1. Connect the test tool to the VIDEO output of the TV Signal Generator as shown in Figure 4-8.

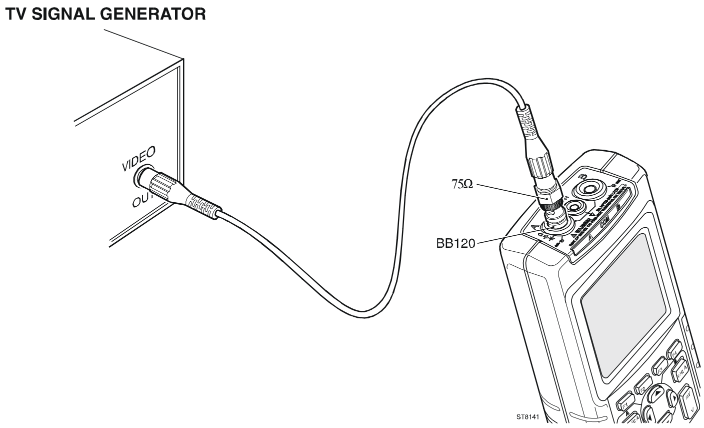


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Figure 4-8. Test Tool Input A to TV Signal Generator

2. Select the following test tool setup:

- Reset the test tool (power off and then on with [power key]).
- Press [SCOPE MENU] to open the SCOPE INPUTS menu.
- Press [F3] to open the TRIGGER menu and choose:

  ■ VIDEO on A...

  From the shown VIDEO TRIGGER menu choose:

  SYSTEM: ■ NTSC or **■ PAL** or **■ SECAM**

  LINE: ■ SELECT

  POLARITY: ■ POSITIVE

- Using [mV] [V] set the Input A sensitivity to 200 mV/div.

- Using s TIME ns select 20 µs/div.
- Press F3 to enable the arrow keys for selecting the video line number.
- Using the up/down arrow keys select the line number:

  622 for PAL or SECAM

  525 for NTSC.

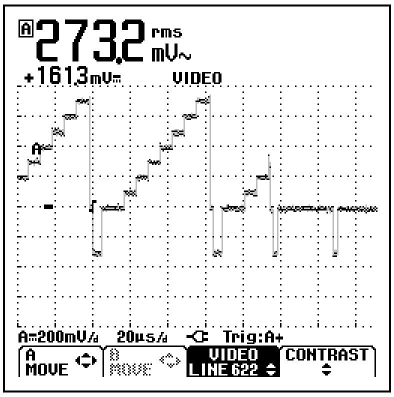
3. Set the TV Signal Generator to source a signal with the following properties:
   - the system selected in step 2
   - gray scale
   - video amplitude 1V (5 divisions on the test tool)
   - chroma amplitude zero.
4. Observe the trace, and check to see if the test tool triggers on line number:

   622 for PAL or SECAM, see Figure 4-9

   525 for NTSC, see Figure 4-10.

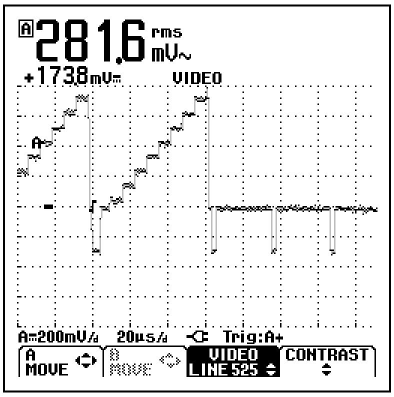
Note

***Numerical readings** in the pictures shown below may deviate from those shown in the test tool display during verification.*



PAL622.BMP

Figure 4-9. Test Tool Screen for PAL/SECAM line 622



NTSC525.BMP

Figure 4-10. Test Tool Screen for NTSC line 525

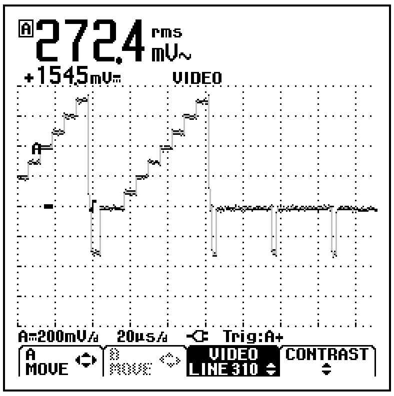
5. Using the up/down arrow keys select the line number:

   310 for PAL or SECAM

   262 for NTSC
6. Observe the trace, and check to see if the test tool triggers on:

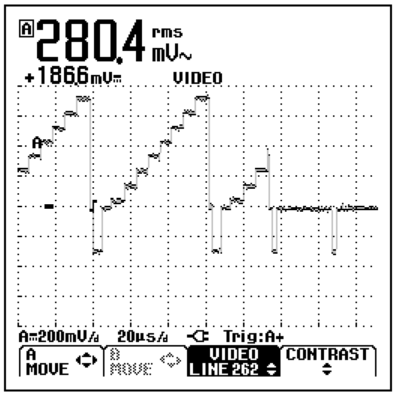
   line number 310 for PAL or SECAM, see Figure 4-11.

   line number 262 for NTSC, see Figure 4-12.



PAL310.BMP

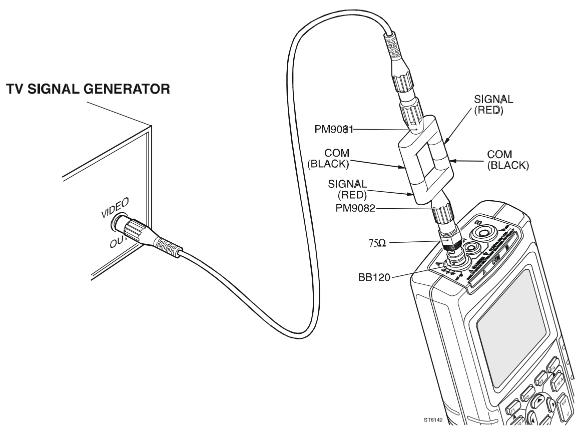
Figure 4-11. Test Tool Screen for PAL/SECAM line 310



NTSC262.BMP

Figure 4-12. Test Tool Screen for NTSC line 262

7. Apply the inverted TV Signal Generator signal to the test tool.
   You can invert the signal by using a Banana Plug to BNC adapter (Fluke PM9081/001) and a Banana Jack to BNC adapters (Fluke PM9082/001), as shown in Figure 4-13.



ST8142.WMF

Figure 4-13. Test Tool Input A to TV Signal Generator Inverted

8. Select the following test tool setup:

   - Press [SCOPE MENU] to open the SCOPE INPUTS menu.
   - Press [F3] to open the TRIGGER menu and choose:

     ■ VIDEO on A

     The VIDEO TRIGGER sub-menu is shown now. From the VIDEO TRIGGER menu choose:

     SYSTEM: ■ NTSC or **■ PAL** or **■ SECAM** or **■ PALplus |**

     LINE: ■ SELECT |

   - **POLARITY: ■ NEGATIVE**
   - Using [mV] [V] set the Input A sensitivity to 200 mV/div.
   - Using [s TIME ns] select 20 µs/div.

9. Using (up/down arrow keys) select the line number:

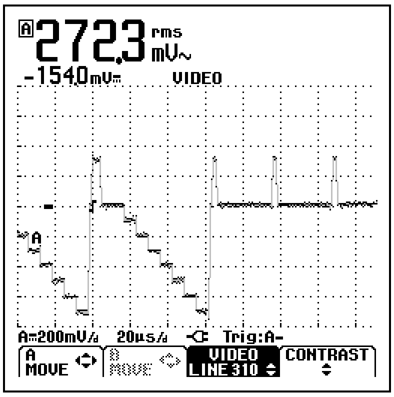
   310 for PAL or SECAM

   262 for NTSC

10. Observe the trace, and check to see if the test tool triggers on:

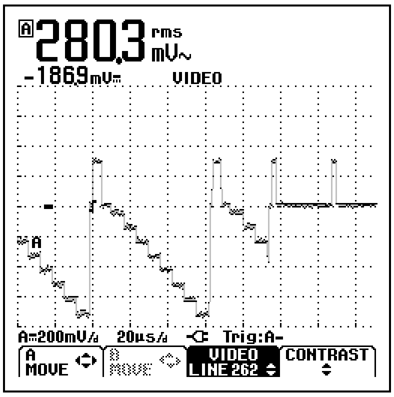
    line number 311 for PAL or SECAM, see Figure 4-14

    line number 262 for NTSC, see Figure 4-15.



PAL310I..BMP

Figure 4-14. Test Tool Screen for PAL/SECAM line 310 Negative Video



NTSC262I.BMP

Figure 4-15. Test Tool Screen for NTSC line 262 Negative Video

This is the end of the Performance Verification Procedure.

Chapter 5
Calibration Adjustment

Title **Page**

5.1 General

5.1.1 Introduction

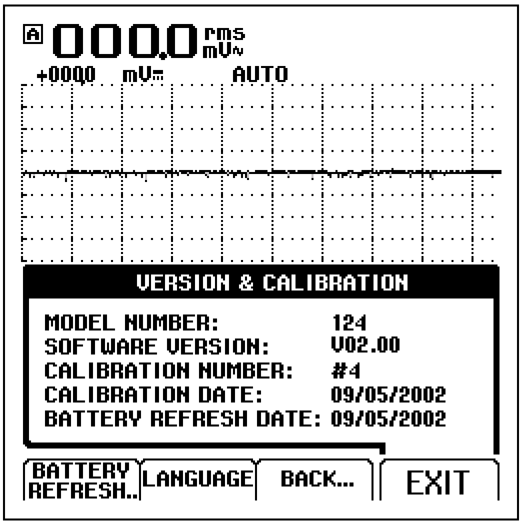
The following information, provides the complete Calibration Adjustment procedure for the Fluke 123 and 124 test tools with **firmware V02.00** and onwards.
The test tool allows closed-case calibration using known reference sources. It measures the reference signals, calculates the correction factors, and stores the correction factors in RAM. After completing the calibration, the correction factors can be stored in FlashROM.

The test tool should be calibrated after repair, or if it fails the performance test. The test tool has a normal calibration cycle of one year. The Calibration Adjustment procedure is identical for Fluke 123 and Fluke 124.

5.1.2 Calibration number and date

When storing valid calibration data in FlashROM after performing the calibration adjustment procedure, the calibration date is set to the actual test tool date, and calibration number is raised by one. To display the calibration date and - number:

1. Press [USER OPTIONS] to open the USER OPTIONS menu.
2. Press [F3] to show the VERSION&CALIBRATION screen (see Figure 5.1).
3. Press [F4] to return to normal mode.



VERSION.BMP

Figure 5-1. Version & Calibration Screen

5.1.3 General Instructions

Follow these general instructions for all-calibration steps:

- Allow the 5500A to satisfy its specified warm-up period. For each calibration point , wait for the 5500A to settle.
- The required warm up period for the test tool is included in the WarmingUp & PreCal calibration step.

- Ensure that the test tool battery is charged sufficiently.

5.2 Equipment Required For Calibration

The primary source instrument used in the calibration procedures is the Fluke 5500A. If a 5500A is not available, you can substitute another calibrator as long as it meets the minimum test requirements.

- Fluke 5500A Multi Product Calibrator, including 5500A-SC Oscilloscope Calibration Option.
- Stackable Test Leads (4x), supplied with the 5500A.
- 50Ω Coax Cables (2x), Fluke PM9091 or PM9092.
- 50Ω feed through terminations (2x), Fluke PM9585.
- Fluke BB120 Shielded Banana to Female BNC adapters (2x), supplied with the Fluke 123/124.
- Dual Banana Plug to Female BNC Adapter (1x), Fluke PM9081/001.
- Male BNC to Dual Female BNC Adapter (1x), Fluke PM9093/001.

5.3 Starting Calibration Adjustment

Follow the steps below to start calibration adjustments.

1. Power the test tool via the power adapter input, using the PM8907 power adapter.
2. Check the actual test tool date, and adjust the date if necessary:
   - Press USER OPTIONS to open the USER OPTIONS menu
   - Using ▲▼ select DATE ADJUST
   - press F4 to open the DATE ADJUST menu
   - adjust the date if necessary.
3. Select the Maintenance mode.

   The Calibration Adjustment Procedure uses built-in calibration setups, that can be accessed in the Maintenance mode.

   To enter the Maintenance mode proceed as follows:

   - Press and hold ☼
   - Press and release F4
   - Release ☼
   - The display shows the Calibration Adjustment Screen.

   The display shows the first calibration step **Warming Up (CL 0200)** , and the calibration status **:IDLE (valid)** or **:IDLE (invalid)**.

4. Continue with either a. or b. below:
   a. To calibrate the display contrast adjustment range and the default contrast, go to Section 5.4 Contrast Calibration Adjustment.
   This calibration step is only required if the display cannot made dark or light enough, or if the display after a test tool reset is too light or too dark.
   b. To calibrate the test tool without calibrating the contrast , go to Section 5.5 Warming Up & Pre-calibration.

Explanation of screen messages and key functions.

When the test tool is in the Maintenance Mode, only the F1 to F4 soft keys, the ON/OFF key, and the backlight key can be operated, unless otherwise stated.

The calibration adjustment screen shows the actual calibration step (name and number) and its status :

Cal Name (CL nnnn) :Status Calibration step nnnn

Status can be:

IDLE (valid)	After (re)entering this step, the calibration process is not started. The calibration data of this step are valid. This means that the last time this step was done, the calibration process was successful. It does not necessarily mean that the unit meets the specifications related to this step!
IDLE (invalid)	After (re)entering this step, the calibration process is not started. The calibration data are invalid. This means that the unit will not meet the specifications if the calibration data are saved.
BUSY aaa% bbb%	Calibration adjustment step in progress; progress % for Input A and Input B.
READY	Calibration adjustment step finished.
Error :xxxx	Calibration adjustment failed, due to wrong input signal(s) or because the test tool is defective. The error codes xxxx are shown for production purposes only.

Functions of the keys F1-F4 are:

F1	PREV	select the previous step
F2	NEXT	select the next step
F3	CAL	start the calibration adjustment of the actual step
F4	EXIT	leave the Maintenance mode

Readings and traces

After completing a calibration step, readings and traces are shown using the new calibration data.

5.4 Contrast Calibration Adjustment

After entering the Maintenance mode, the test tool display shows
Warming Up (CL 0200):IDLE (valid).
Do not press F3 now! If you did, turn the test tool off and on, and enter the Maintenance mode again.

Proceed as follows to adjust the maximum display darkness (CL0100), the default contrast (CL0110) , and the maximum display brightness (CL0120).

1. Press F1 a three times to select the first calibration step. The display shows:
   Contrast (CL 0100) :MANUAL
2. Press F3 CAL. The display will show a dark test pattern, see Figure 5-2
3. Using ▲▼ adjust the display to the maximum darkness, at which the test pattern is only just visible.
4. Press F2 to select the default contrast calibration. The display shows:
   Contrast (CL 0110) :MANUAL
5. Press F3 CAL. The display shows the test pattern at default contrast.
6. Using ▲▼ set the display to optimal (becomes default) contrast.
7. Press F2 to select maximum brightness calibration. The display shows:
   Contrast (CL 0120) :MANUAL
8. Press F3 CAL. The display shows a bright test pattern.
9. Using ▲▼ adjust the display to the maximum brightness, at which the test pattern is only just visible.
10. You can now :
    - Exit, if only the Contrast had to be adjusted. Continue at Section 5.7.

    OR

    - Do the complete calibration. Press F2 to select the next step (Warming Up), and continue at Section 5.5.

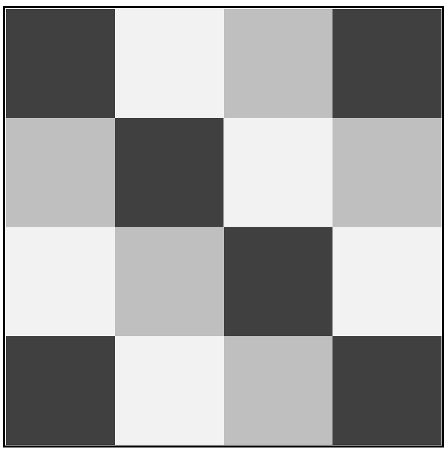


Figure 5-2. Display Test Pattern

5.5 Warming Up & Pre-Calibration

After entering the Warming-Up & Pre-Calibration state, the display shows:
WarmingUp (CL 0200):IDLE (valid) or **(invalid)**.

You must always start the Warming Up & Pre Calibration at **Warming Up (CL0200)** . Starting at another step will make the calibration invalid!

Proceed as follows:

1. Remove all input connections from the test tool.
2. Press F3 to start the Warming-Up & Pre-Calibration.
   The display shows the calibration step in progress, and its status.
   The first step is **WarmingUp (CL0200) :BUSY 00:29:59 .** The warming-up period is counted down from 00:29:59 to 00:00:00. Then the other pre-calibration steps are performed automatically. The procedure takes about 60 minutes.
3. Wait until the display shows **End Precal :READY**
4. Continue at Section 5.6.

5.6 Final Calibration

You must always start the Final Calibration at the first step of Section 5.6.1. Starting at another step will make the calibration invalid!

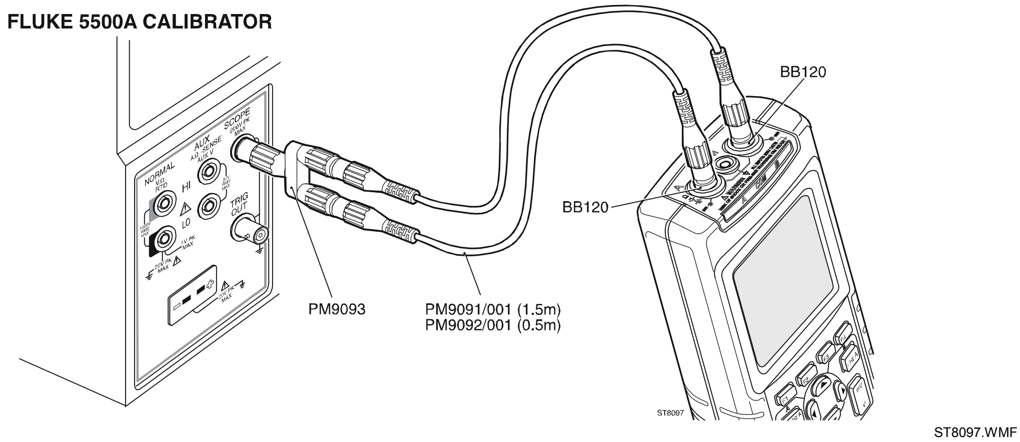
If you proceeded to step N (for example step CL 0615), then return to a previous step (for example step CL 0613) , and then calibrate this step, the complete final calibration becomes invalid. You must do the final calibration from the beginning (step CL 0600) again.

You can repeat a step that shows the status **:READY** by pressing F3 again.

5.6.1 HF Gain Input A&B

Proceed as follows to do the HF Gain Input A&B calibration:

1. Press F2 to select the first calibration step in Table 5-1 (**HFG & FI AB (CL 0600):**)
2. Connect the test tool to the 5500A as shown in Figure 5-3. Do NOT use 50Ω terminations!



ST8097.WMF

Figure 5-3. HF Gain Calibration Input Connections

3. Set the 5500A to source a 1 kHz fast rising edge square wave (Output SCOPE, MODE edge) to the first calibration point in Table 5-1.
4. Set the 5500A in operate (OPR).
5. Press F3 to start the calibration.
6. Wait until the display shows calibration status **READY** .
7. Press F2 to select the next calibration step, set the 5500A to the next calibration point, and start the calibration. Continue through all calibration points in Table 5-1.
8. Set the 5500A to source a 1 kHz square wave (Output SCOPE, MODE wavegen, WAVE square), to the first calibration point in Table 5-2.
9. Press F2 to select the first step in Table 5-2.
10. Press F3 to start the calibration.
11. Wait until the display shows calibration status **READY**.
12. Press F2 to select the next calibration step, set the 5500A to the next calibration point, and start the calibration. Continue through all calibration points Table 5-2.
13. When you are finished, set the 5500A to Standby.
14. Continue at Section 5.6.2.

Table 5-1. HF Gain Calibration Points Fast

Cal step	**5500A Setting** 1) (1 kHz, no 50Ω!)	**Test Tool Input Signal Requirements** 1) (1 kHz, t_{rise}<100 ns, flatness after rising edge: <0.5% after 200 ns)
HFG & FI AB (CL 0600)	10 mV	20 mV
HFG & FI AB (CL 0601)	25 mV	50 mV
HFG & FI AB (CL 0602)	50 mV	100 mV
HFG & FI AB (CL 0603)	100 mV	200 mV
HFG & FI AB (CL 0604)	250 mV	500 mV
HFG & FI AB (CL 0605)	500 mV	1V
HFG & FI AB (CL 0606)	1V	2V
HFG & FI AB (CL 0607) [HFG & FI A (CL 0608), HFG & FI B (CL 0628)] 2)	2.5V	5V

1) As the 5500A output is not terminated with 50Ω, its output voltage is two times its set voltage

2) After starting the first step in this table cell, these steps are done automatically.

Table 5-2. HF Gain Calibration Points Slow

Cal step	**5500A Setting** (1 kHz, MODE wavegen, WAVE square)	**Test Tool Input Signal Requirements** (1 kHz square, t_{rise}<2 µs, flatness after rising edge: <0.5% after 4 µs)
HF-Gain AB (CL 0609)	25V	25V
HF-Gain A (CL 0612), HF-Gain B (CL 0632) HF-Gain A (CL 0615), HF-Gain B (CL 0635)] 1)	50V	50V

1) After starting the first step in this table cell, these steps are done automatically.

5.6.2 Delta T Gain, Trigger Delay Time & Pulse Adjust Input A

Proceed as follows to do the calibrations:

1. Press F2 to select calibration step **Delta T (CL 0700):IDLE**
2. Connect the test tool to the 5500A as shown in Figure 5-4.

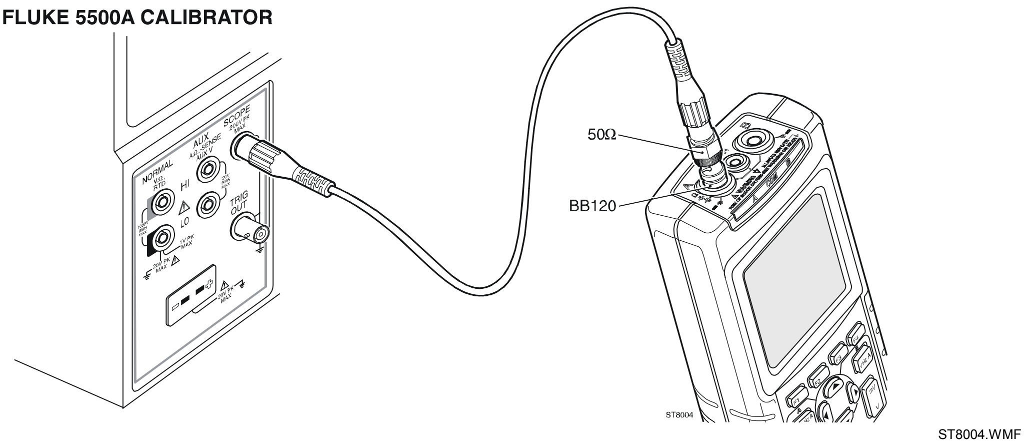


Figure 5-4. 5500A Scope Output to Input A

3. Set the 5500A to source a 1V, 1 MHz fast rising (rise time ≤ 1 ns) square wave (SCOPE output, MODE edge).
4. Set the 5500A to operate (OPR).
5. Press F3 to start the calibration.
   The Delta T gain, Trigger Delay (CL0720), and Pulse Adjust Input A (CL0640) will be calibrated.
6. Wait until the display shows **Pulse Adj A (CL 0640):READY**.
7. When you are finished, set the 5500A to Standby.
8. Continue at Section 5.6.3.

5.6.3 Pulse Adjust Input B

Proceed as follows to do the Pulse Adjust Input A calibration:

1. Press F2 to select calibration step **Pulse Adj B (CL 0660):IDLE**
2. Connect the test tool to the 5500A as shown in Figure 5-5.

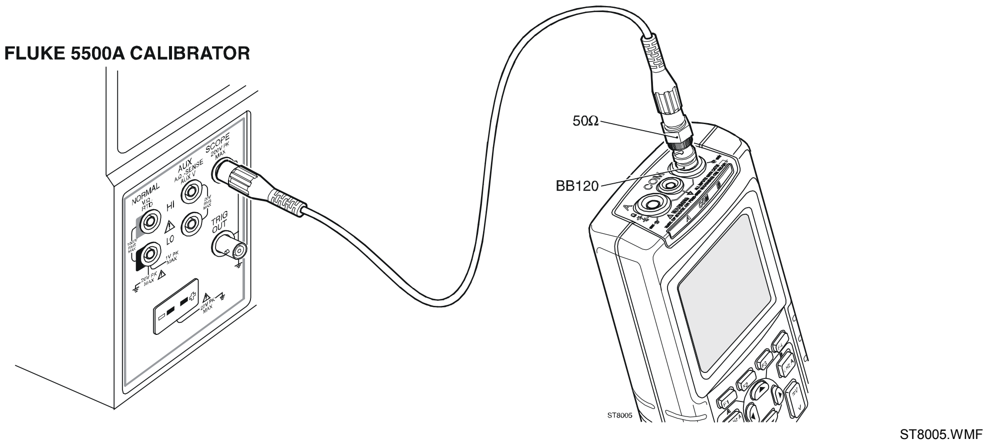


Figure 5-5. 5500A Scope Output to Input B

3. Set the 5500A to source a 1V, 1 MHz fast rising square wave (SCOPE output, MODE edge) (rise time ≤ 1 ns, aberrations <2% pp).
4. Set the 5500A to operate (OPR).
5. Press F3 to start the calibration.
6. Wait until the display shows **Pulse Adj B (CL 0660):READY**.
7. When you are finished, set the 5500A to Standby.
8. Continue at Section 5.6.4.

5.6.4 Gain DMM (Gain Volt)

Warning

Dangerous voltages will be present on the calibration source and connection cables during the following steps. Ensure that the calibrator is in standby mode before making any connection between the calibrator and the test tool.

Proceed as follows to do the Gain DMM calibration.

1. Press F2 to select the first calibration step in Table 5-3.
2. Connect the test tool to the 5500A as shown in Figure 5-6.

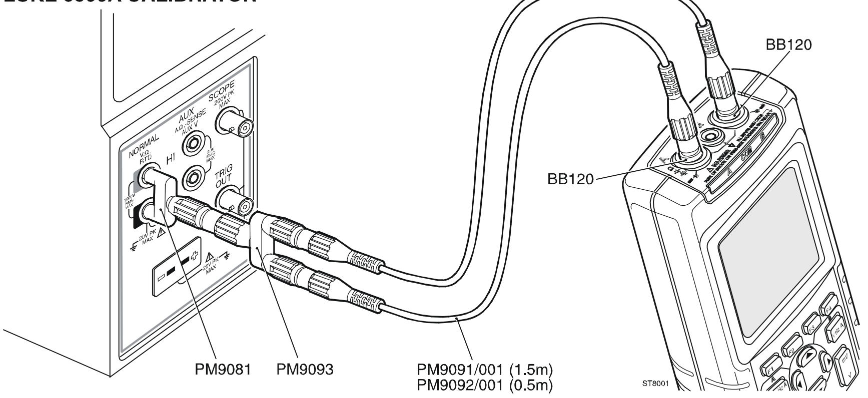


Figure 5-6. Volt Gain Calibration Input Connections <300V

3. Set the 5500A to supply a DC voltage, to the first calibration point in Table 5-3.
4. Set the 5500A to operate (OPR).
5. Press F3 to start the calibration.
6. Wait until the display shows calibration status **:READY**.
7. Press F2 to select the next calibration step, set the 5500A to the next calibration point, and start the calibration. Continue through all calibration points of Table 5-3
8. Set the 5500A to Standby, and continue with step 9.

Table 5-3. Volt Gain Calibration Points <300V

Cal step	Input value
Gain DMM (CL0800)	12.5 mV
Gain DMM (CL0801)	25 mV
Gain DMM (CL0802)	50 mV
Gain DMM (CL0803)	125 mV
Gain DMM (CL0804)	250 mV
Gain DMM (CL0805)	500 mV
Gain DMM (CL0806)	1.25V
Gain DMM (CL0807)	2.5V
Gain DMM (CL0808)	5V
Gain DMM (CL0809)	12.5V
Gain DMM (CL0810)	25V
Gain DMM (CL0811)	50V (set 5500A to OPR!)
Gain DMM (CL0812)	125V
Gain DMM (CL0813)	250V

9. Press F2 to select calibration step **Gain DMM (CL0814) :IDLE**

10. Connect the test tool to the 5500A as shown in Figure 5-7.

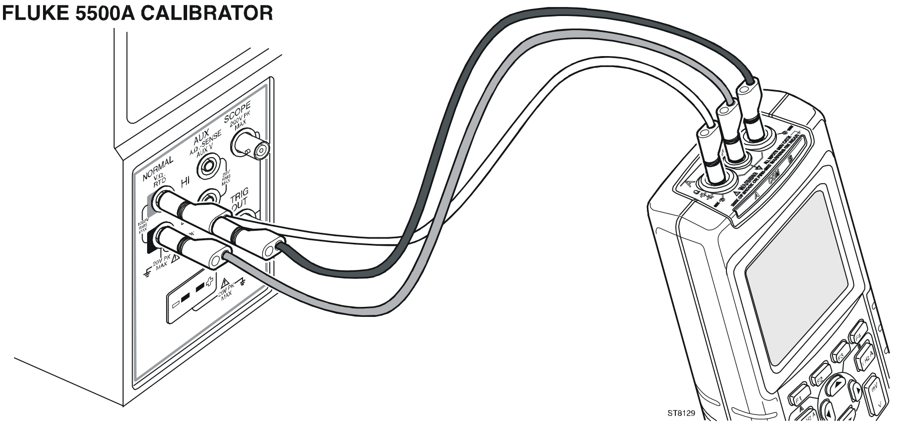


Figure 5-7. Volt Gain Calibration Input Connections 500V

11. Set the 5500A to supply a DC voltage of 500V.
12. Set the 5500A to operate (OPR).
13. Press F3 to start the calibration.
    Gain DMM (CL0814) and Gain DMM (CL0815) will be calibrated now.
14. Wait until the display shows calibration status **Gain DMM (CL0815):READY**.
15. Set the 5500A to 0V (zero) and to Standby.
16. Continue at Section 5.6.5.

5.6.5 Volt Zero

Proceed as follows to do the Volt Zero calibration:

1. Press F2 to select calibration adjustment step **Volt Zero (CL 0820):IDLE**.
2. Terminate Input A and Input B with the BB120 and a 50Ω or lower termination.
3. Press F3 to start the zero calibration of all mV/d settings (CL0820...CL0835)
4. Wait until the display shows **Volt Zero (CL 0835):READY**.
5. Remove the 50Ω terminations from the inputs.
6. Continue at Section 5.6.6.

5.6.6 Zero Ohm

Proceed as follows to do the Zero Ohm calibration:

1. Press F2 to select calibration adjustment step **Zero Ohm (CL 0840):IDLE**
2. Make a short circuit between the Input A banana socket and the COM input .
3. Press F3 to start the Ohm Zero calibration of all ranges (CL 0840...CL 0846).
4. Wait until the display shows the calibration status **Zero Ohm (CL 0846):READY**.
5. Remove the Input A to COM short.
6. Continue at Section 5.6.7.

5.6.7 Gain Ohm

Proceed as follows to do the Gain Ohm calibration:

1. Press F2 to select calibration adjustment step **Gain Ohm (CL 0860):IDLE**
2. Connect the UUT to the 5500A as shown in Figure 5-8.
   Notice that the sense leads must be connected directly to the test tool.

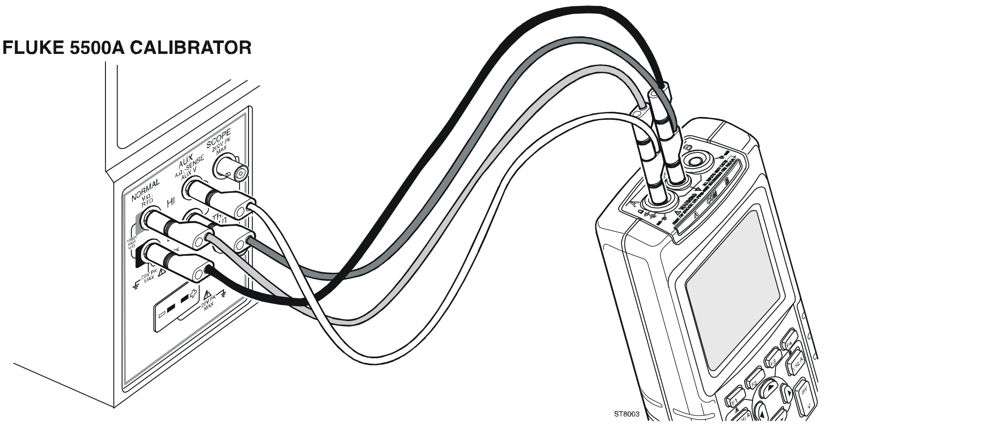


Figure 5-8. Four-wire Ohms calibration connections

3. Set the 5500A to the first test point in Table 5-4. Use the 5500A “COMP 2 wire” mode for the calibration adjustments up to and including 100 kΩ. For the higher values, the 5500A will turn off the “COMP 2 wire” mode.
4. Set the 5500A to operate (OPR).
5. Press F3 to start the calibration.
6. Wait until the display shows the calibration status **:READY**.
7. Press F2 to select the next calibration step, set the 5500A to the next calibration point, and start the calibration. Continue through all calibration points.
8. When you are finished, set the 5500A to Standby.
9. Continue at Section 5.6.8.

Table 5-4. Ohm Gain Calibration Points

Cal Step	Input Value
Gain Ohm (CL 0860) [Cap. Pos. (CL 0920), Cap.Neg. (CL 0921)][1)]	100Ω
Gain Ohm (CL 0861) [Cap. Pos. (CL 0922), Cap.Neg. (CL 0923)][1)]	1 kΩ
Gain Ohm (CL 0862) [Cap. Pos. (CL 0924), Cap.Neg. (CL 0925)][1)]	10 kΩ
Gain Ohm (CL 0863) [Cap. Pos. (CL 0926), Cap.Neg. (CL 0927)][1)]	100 kΩ
Gain Ohm (CL 0864)	1 MΩ
Gain Ohm (CL 0865) [Gain Ohm (CL 0866)][2)]	10 MΩ

1) The capacitance measurement current calibrations (Cap.Pos. and Cap.Neg) are done automatically after the Gain Ohm calibration.
2) The Gain Ohm (CL0866) calibration step is done automatically after the Gain Ohm (CL0865) calibration.

5.6.8 Capacitance Gain Low and High

Proceed as follows to do the Capacitance Gain calibration:

1. Press F2 to select calibration adjustment step **Cap. Low (CL 0900):IDLE**
2. Connect the test tool to the 5500A as shown in Figure 5-9.

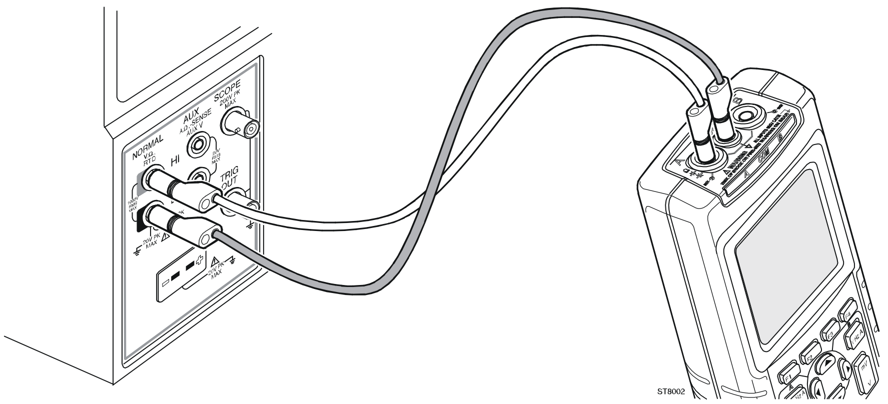


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Figure 5-9. Capacitance Gain Calibration Input Connections

3. Set the 5500A to supply 250 mV DC.
4. Set the 5500A to operate (OPR).
5. Press F3 to start the calibration.
6. Wait until the display shows **Cap. Low (CL 0900):READY**.
7. Press F2 to select calibration adjustment step **Cap. High (CL 0910):IDLE**
8. Set the 5500A to supply 50 mV DC.
9. Press F3 to start the calibration.
10. Wait until the display shows **Cap High (CL 910):READY**.
11. Set the 5500A to Standby.
12. Continue at Section 5.6.9.

5.6.9 Capacitance Clamp & Zero

Proceed as follows to do the Capacitance Clamp Voltage & Zero calibration:

1. Press F2 to select calibration adjustment step **Cap. Clamp (CL 0940):IDLE**
2. Remove any input connection from the test tool (open inputs).
3. Press F3 to start the calibration.
   The capacitance measurement clamp voltage **Cap. Clamp (CL 0940),** and the zero of the capacitance ranges **Cap. Zero (CL 0950)**... **Cap. Zero (CL 0953)** will be calibrated now.
4. Wait until the display shows **Cap. Zero (CL 0953): READY**.
5. Continue at Section 5.6.10.

5.6.10 Capacitance Gain

Proceed as follows to do the Capacitance Gain calibration:

1. Press F2 to select calibration adjustment step **Cap. Gain (CL 0960):IDLE**
2. Connect the test tool to the 5500A as shown in Figure 5-9 (Section 5.6.8).
3. Set the 5500A to 500 nF.
4. Set the 5500A to operate (OPR).
5. Press F3 to start the calibration.
6. Wait until the display shows **Cap. Gain (CL 0960):READY**.
7. Continue at Section 5.7 to save the calibration data.

5.7 Save Calibration Data and Exit

Proceed as follows to save the calibration data, and to exit the Maintenance mode:

1. Remove all test leads from the test tool inputs. Do NOT turn off the test tool!
2. Press F4 (EXIT). The test tool will display:

Calibration data is valid **Save data and EXIT maintenance?**

Note

Calibration data valid indicates that the calibration adjustment procedure is performed correctly. It does not indicate that the test tool meets the characteristics listed in Chapter 2.

4. Press F4 (YES) to save and exit.

Notes

- *The calibration number and date will be updated only if the calibration data have been changed and the data are valid.*
- *The calibration data will change when a calibration adjustment has been done. The data will not change when just entering and then leaving the maintenance mode without doing a calibration adjustment.*
- *The calibration number and date will NOT be updated if only the display contrast has been adjusted.*

Possible error messages.

The following messages can be shown on the test tool display:

WARNING.Calibration data NOT valid. **Save data and EXIT?**

Proceed as follows:

- To return to the Maintenance mode:

  Press F3 NO.

  Now press F1 until the display shows **WarmingUp (CL 0200):IDLE**, and calibrate the test tool, starting at Section 5.5.

- To exit and save the INVALID calibration data:

  Press F4 YES.

The test tool will show the message **The test tool needs calibration. Please contact your service center** at power on. The calibration date and number will not be updated. A complete recalibration must be done.

- To exit and maintain the old calibration data:

  Turn the test tool off.

WARNING.No adapter present. **Calibration data will not be saved.** **Exit maintenance mode?**

- To save the calibration data:

  Press F3 NO

  The test tool returns to the maintenance mode. Then supply the correct adapter input voltage, and press F4 to exit and save.

  - To exit without saving the calibration data:

    Press F4 YES

Chapter 6
Disassembling the Test Tool

Title	Page

6.1. Introduction

This section provides the required disassembling procedures. The printed circuit board removed from the test tool must be adequately protected against damage.

Warning

To avoid electric shock, disconnect test leads, probes and power supply from any live source and from the test tool itself. Always remove the battery pack before completely disassembling the test tool. If repair of the disassembled test tool under voltage is required, it shall be carried out only by qualified personnel using customary precautions against electric shock.

6.2. Disassembling Procedures

6.1.1 Required Tools

To access all the assemblies, you need the following:

- Static-free work surface, and anti-static wrist wrap.
- #8, and #10 Torx screwdrivers.
- Cotton gloves (to avoid contaminating the lens, and the PCA).

6.2.2 Removing the Battery Pack

Referring to Figure 6-1, use the following procedure to remove the battery pack.

1. Loosen the M3 Torx screw (item 15) (do not remove it) from the battery door.
2. Lift the battery door at the screw edge to remove it.
3. Lift out the battery pack, and unplug the cable leading to the Main PCA (pull the cable gently backwards).

6.2.3 Removing the Bail

Referring to Figure 6-1, use the following procedure to remove the bail (item 16).

1. Set the bail to a 45 degree position respective to the test tool bottom.
2. Holding the test tool tight, rotate the bail firmly sideways.

6.2.4 Opening the Test Tool

Referring to Figure 6-1, use the following procedure to open the test tool.

1. Remove the battery pack (see Section 6.2.2)
2. Unscrew the four M3 Torx screws (item 12) that secure the bottom case to the top case.
3. Hold the test tool upside down, and lift off the bottom case.

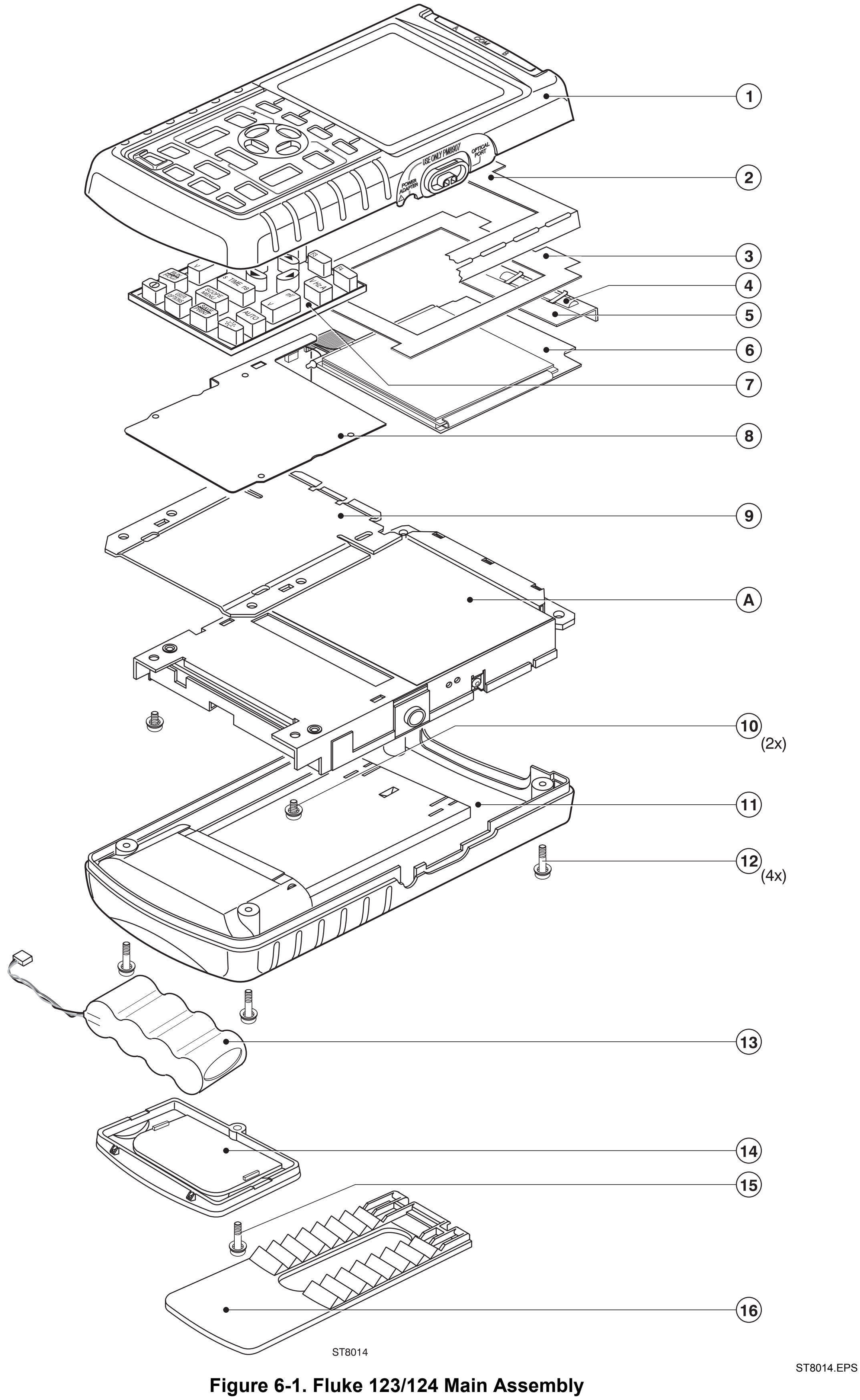


Figure 6-1. Fluke 123/124 Main Assembly

6.2.5 Removing the Main PCA Unit

Referring to Figure 6-1, use the following procedure to remove the main PCA unit.

1. Open the test tool (see Section 6.2.4).
2. Disconnect the LCD flex cable, and the keypad foil flat cable, see Figure 6-2.
   Unlock the cables by lifting the connector latch. The latch remains attached to the connector body.
   The keypad foil is provided with a shielding flap that covers the LCD flat cable. The end of the flap is put under the main PCA unit shielding plate, and can be easily pulled out.

Caution

To avoid contaminating the flex cable contacts with oil from your fingers, do not touch the contacts (or wear gloves). Contaminated contacts may not cause immediate instrument failure in controlled environments. Failures typically show up when contaminated units are operated in humid areas.

3. Unplug the backlight cable.

Warning

If the battery pack or the power adapter is connected, the LCD backlight voltage on the wire cable is 400V ! (when the test tool is on).

4. Remove the two screws (item 10) that secure the Main PCA unit to the top case.
5. Lift the screw end of the Main PCA unit and remove the unit by gently wiggling the assembly from side to side as you pull backwards.

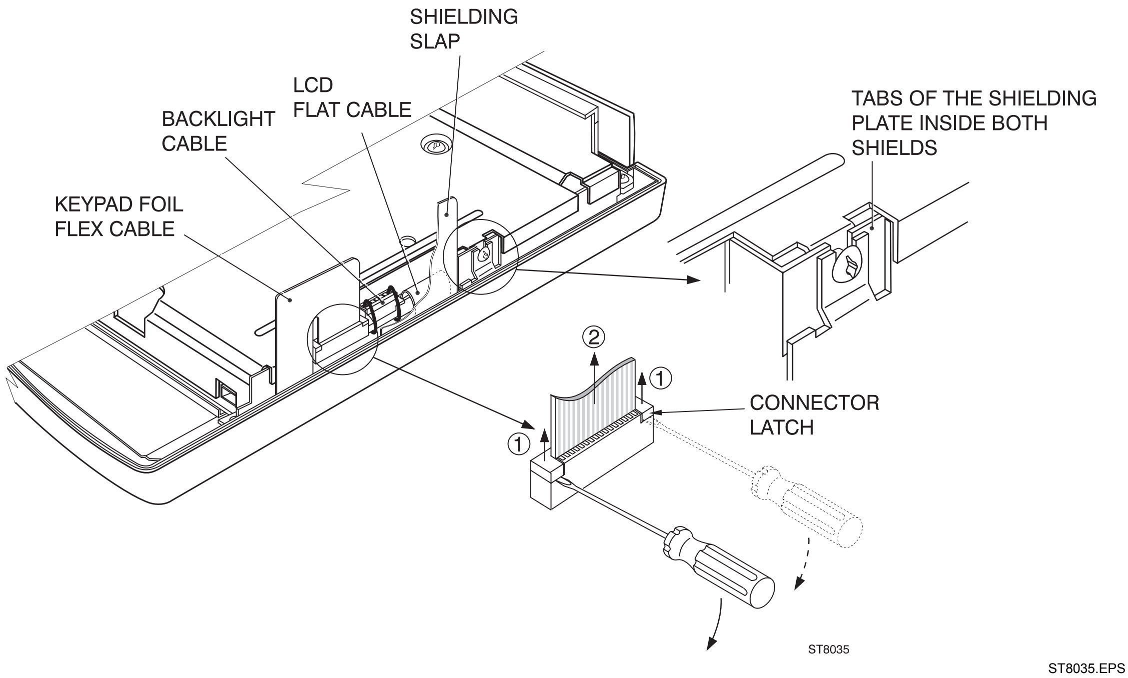


Figure 6-2. Flex Cable Connectors

6.2.6 Removing the Display Assembly

Caution

Read the Caution statement in Section 6.5 when installing the display assembly. An incorrect installation can damage the display assembly.

There are no serviceable parts in the display assembly. Referring to Figure 6-1, use the following procedure to remove the display assembly.

1. Remove the main PCA unit (see Section 6.2.5).
2. The keypad pressure plate (item 9) is captivated by four plastic keeper tabs in the top case. Press the plate down, carefully slide the plate to release it from the tabs, and then remove it.
3. Remove the display assembly (item 6). To prevent finger contamination, wear cotton gloves, or handle the display assembly by its edge.

After removing the display assembly, the shielding bracket (item 5) with the conductive foam strip (item 4), the dust seal (item 3), and the shielding foil (item 2) can be removed.

6.2.7 Removing the Keypad and Keypad Foil

Referring to Figure 6-1, use the following procedure to remove the keypad and the keypad foil.

1. Remove the display assembly (see Section 6.2.6).
2. Remove the keypad foil. Notice the four keypad foil positioning pins in the top case.
3. Remove the keypad.

Caution

To avoid contaminating the keypad contacts, and the keypad foil contacts with oil from your fingers, do not touch the contacts (or wear gloves). Contaminated contacts may not cause immediate instrument failure in controlled environments. Failures typically show up when contaminated units are operated in humid areas.

6.3 Disassembling the Main PCA Unit

Referring to Figure 6-3, use the following procedure disassemble the main PCA unit.

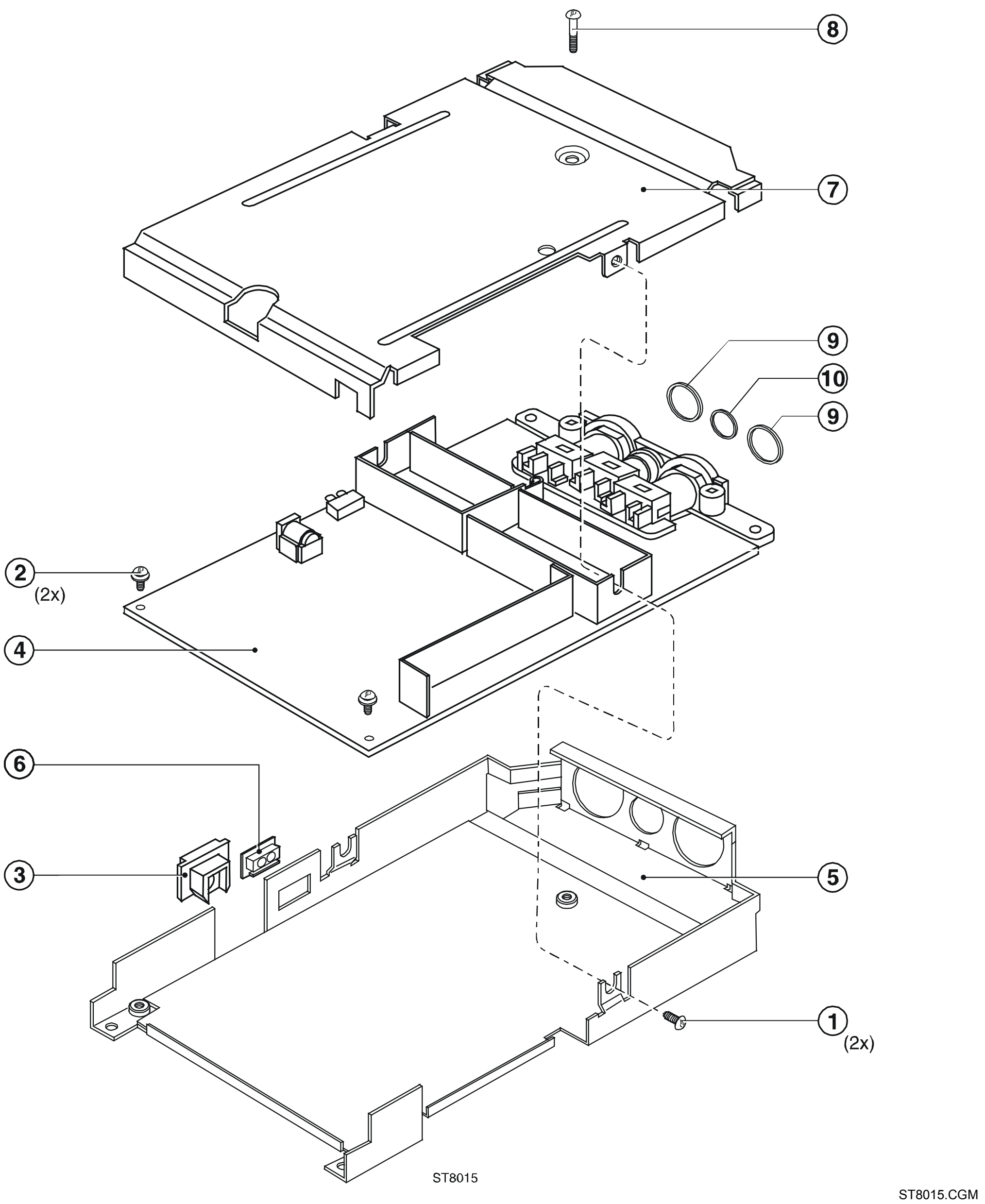
1. Remove the M2.5 Torx screws (items 1 and 8) that secure the main shielding plate (item 7) to the main PCA shielding box (item 5).
2. Pull the shielding plate away from the input banana jacks as you rotate the far end upwards, and then remove it.
3. Remove the power input insulator (item 3), and the LED guide piece (item 6).
4. Remove the M2.5.Torx screws (item 2) that secure the PCA to the shielding box.
5. Lift the PCA at the screw end approximately 2 cm, and pull it away from the input banana jack holes to remove it.

Note

Each input banana jacket is provided with a rubber sealing ring (Input A,B item 9, COM input item 10). Ensure that the rings are present when reassembling the main PCA unit!

Caution

To avoid contaminating the main PCA with oil from your fingers, do not touch the contacts (or wear gloves). A contaminated PCA may not cause immediate instrument failure in controlled environments. Failures typically show up when contaminated units are operated in humid areas.



6-3. Main PCA Unit Assembly

6.4 Reassembling the Main PCA Unit

Reassembling the main PCA is the reverse of disassembly. However you must follow special precautions when reassembling the main PCA unit.

1. Ensure the input banana jacks have the rubber sealing ring in place (Input A, B item 9, COM input item 10, see Figure 4-6).
2. Do not forget to install the power connector insulator (item 3) and the LED holder (item 6).
3. Notice the correct position of the shielding box, main PCA (notice the shielding plates on the PCA), and shielding plate, as shown in Figure 6-2. The tabs of the shielding plate must be inside both shields.

6.5 Reassembling the Test Tool

Reassembling the test tool is the reverse of disassembly. However you must follow special precautions when reassembling the test tool. Refer also to figure 6-1.

Caution

The first shipped units are provided with a yellow tube on the two notches with the screw inserts at the top in the top case,. The reason for this is that the display assembly in these units is smaller than in the later units. All display assemblies supplied as spare part are of the latest type, and do not need the yellow tubes in the top case.

- **Remove the tube from both notches when installing a new display assembly!**
- **Transfer the tubes to the new top case, if you replace a top case that has the tubes installed, and you re-install the unit's original display assembly.**

Reassembling procedure for a completely disassembled unit:

1. Clean the inside of the lens with a moist soft cloth if necessary. Keep the lens free of dust and grease.
2. Install the keypad. Press the edge of the keypad into the sealing groove of the top case. Ensure that the keypad lays flat in the top case, and that all keys are correctly seated.
3. Install the shielding foil (item 2). Remove the protection foil from the shielding foil, by pulling it off in one rapid movement! If you pull it off slowly, the protection foil may crack. Keep the shielding foil free of dust and grease.
4. Install the dust seal (item 3).
5. Install the display shielding bracket (item 5) provided with the conductive foam strip (item 4).

Note

Figure 6-4 shows how the shielding bracket (with conductive foam strip), the shielding foil, the dust seal, and the display assembly (see step 7) are clamped in the top cover edge.

6. Install the keypad foil. Align the positioning holes in the keypad foil to the positioning pins in the top case.

7. Clean the display glass with a moist soft cloth if necessary. Install the display assembly. Ensure that the display is secured correctly by the four alignment tabs in the top case. It is secured correctly when it cannot be moved horizontally.
8. Install the keypad pressure plate. Press the plate firmly, and slide it under the four plastic keeper tabs in the top case.
9. Install the main PCA unit, and re-attach the cables. Secure the flat cables in the connectors with the connector latches. **Keep the backlight wires twisted to minimize interference voltages!** Insert the shielding flap below the main PCA shielding plate.
10. Put the bottom case and the top case together at the flat cable side, and hinge the cases to each other. This ensures the keypad foil flat cable is folded correctly.
11. Install the battery pack, and the battery door, see figure 6-5.

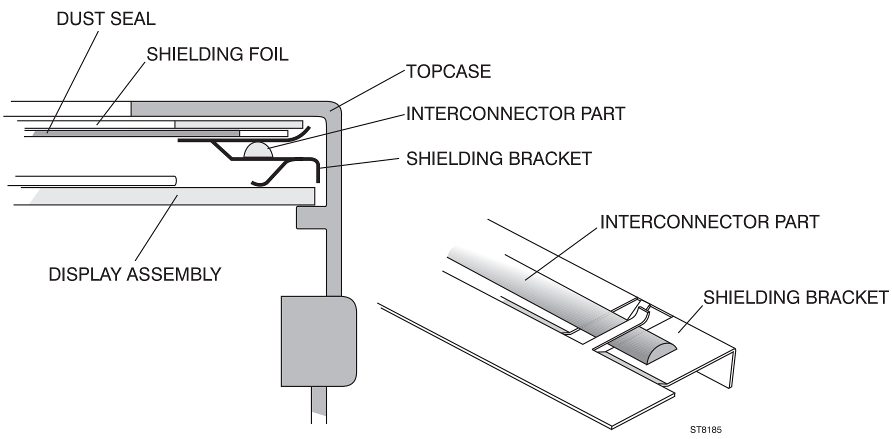


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Figure 6-4. Mounting the display shielding bracket

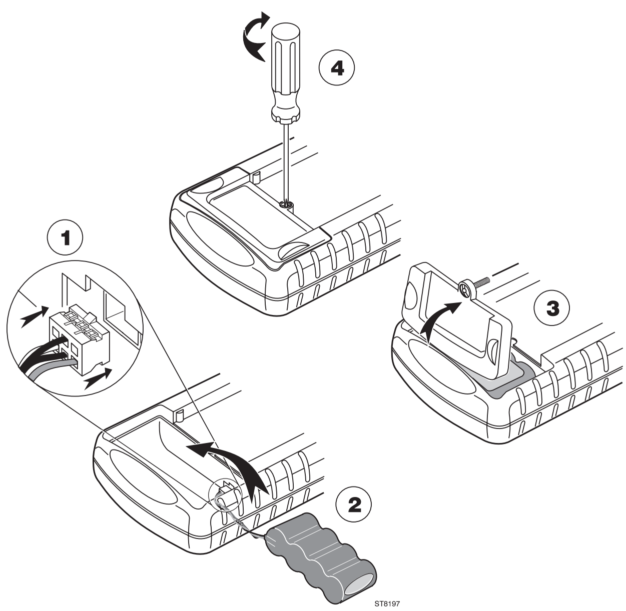

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Figure 6-5. Battery pack installation

Chapter 7
Corrective Maintenance

Title Page

7.1 Introduction

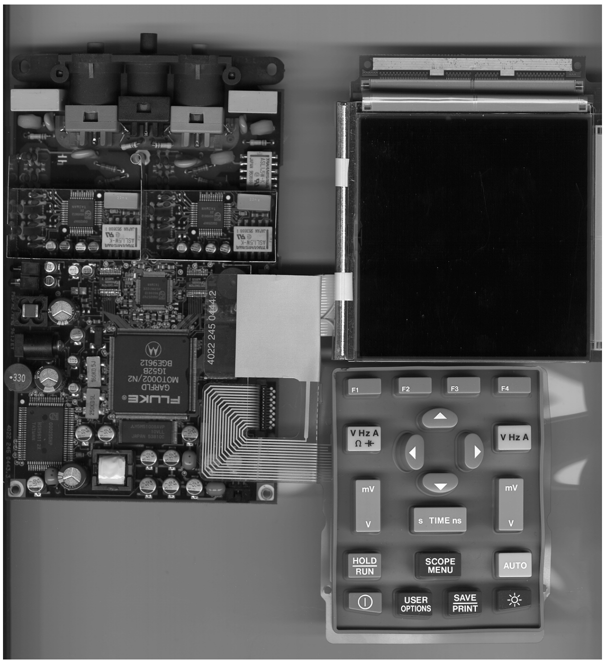
This chapter describes troubleshooting procedures that can be used to isolate problems with the test tool.

Warning

Opening the case may expose hazardous voltages. For example, the voltage for the LCD back light fluorescent lamp is >400V! Always disconnect the test tool from all voltage sources and remove the batteries before opening the case. If repair of the disassembled test tool under voltage is required, it shall be carried out only by qualified personnel using customary precautions against electric shock.

- If the test tool fails, first verify that you are operating it correctly by reviewing the operating instructions in the Users Manual or Getting Started Manual.
- When making measurements for fault finding, you can use the black COM input banana jack, or the metal shielding on the Main PCA unit, as measurement ground.
- To access the Main PCA for measurements, proceed as follows:

1. Remove the Main PCA unit, see Section 6.2.5.
2. Disassemble the Main PCA unit, see Section 6.3.
3. Connect the Display Assembly flat cable, the Backlight cable, and the Keypad Foil flex cable to the Main PCA unit. Position the Keypad on the Keypad foil. See Figure 7.1. The Test tool without the case is operative now.
4. Power the PCA via the Power Adapter and/or battery pack. Watch out for short circuiting due to metal parts on your desk!!



REPAIR3.BMP

Figure 7-1. Operative Test Tool without Case

7.2 Starting Fault Finding.

After each step, continue with the next step, unless stated otherwise.

Power the test tool by the battery pack only, then by the power adapter only.

1. The test tool operates with the power adapter, but not with the battery only: install a charged battery (VBAT >4V), and check the connections between the battery and the test tool (X503, R504, R506, R507).
2. The test tool operates with the battery pack, but not with the power adapter only, and the battery pack is not charged by the test tool: continue at 7.3 Charger Circuit.
3. The test tool operates neither with the battery pack, nor with the power adapter: continue at 7.4 Starting with a Dead Test Tool.
4. Particular functions are not correct: continue at 7.5 Miscellaneous Functions.

Table 7-1. Starting Fault Finding

	Power adapter	Battery Pack	Check
1	OK	NOT OK	Battery pack, connector, sense resistors
2	NOT OK	OK	See Section 7.3 Charger Circuit
3	NOT OK	NOT OK	See Section 7.4 Starting with a Dead Test Tool
4	Partly OK	Partly OK	See Section 7.5 Miscellaneous Functions

7.3 Charger Circuit

1. Power the test tool by the power adapter only.
2. Check TP501 for ≅15...20V.
   If not correct, check the power adapter input circuit (X501, Z501,V501, C501).
3. Check TP504 (VBAT) for about 7.5V.
   If not correct, check R501, V504, V503, L501, C503.
   Check TP502 for a 100 kHz, 13Vpp pulse signal; if correct or low, check if TP504 is shorted to ground, and check V506.
4. Install a charged battery. The voltage at TP504 will be now about 5V.
5. Check N501 pin 18 (P7VCHA) for ≅7V.
   If not correct, check N501 pin 20 for ≅15V (supplied via R502). If 15V on pin 20 is correct, check C507, replace N501.

P7VCHA is the supply voltage for the charger control circuit in N501. It is derived from VADAPTER (pin20), by an internal linear supply in N501.

6. Check N501 pin 12 (NETVALID) for +2.7V, and TP529 (MAINVAL) for +3.3V.

The NETVALID and MAINVAL signals indicate to the P-ASIC and the D-ASIC that a correct power adapter voltage is connected. The signals enable control of the P-ASIC CHARGE circuit (controls V506 by 100 kHz, 13Vpp square wave).

If correct continue at step 7.

If not correct, then:

a. Check TP571 (+3V3GAR) for +3V3V.
If not correct, possibly caused by V569, R580, TP571 short to ground, loose pins of N501, N501 defective.

b. Check N501 pin 8 (VADALOW) for ≅ 1.1V
If not correct:

1. Check R515 and connections.

The P-ASIC supplies a current to R515. The current source uses REFPWM2 and IREF, see 2 and 3 below.

2. Check N501 pin 73 (REFPWM2) for +3V3. REFPWM2 is supplied by the P-ASIC. Check TP307 (N501 pin 72, REFP) for 1.22V, check V301 and R307.

3. Check N501 pin 74 (IREF) for 1.61V.
If not correct, possibly caused by R528, loose pin 74, or N501 defective.

c. Check +3V3SADC on N501 pin 65 for +3.3V.

7. Check TP531 (CHARCURR):

The CHARCURR signal controls the battery charge current.

If TP531 < 2.7V continue at step 7a.
If TP531 >2.7V continue at step 7b.

a. Check if charger FET V506 is controlled by a ≅100 kHz, 13 Vpp square wave on TP502 (FET gate). If correct check/replace V506.
If not correct, check:

1. N501 pin 4 TEMPHI relative to X503 pin 3 (=N501 pin 9) for ≅ 200 mV. If not correct, check R512 and connections.

2. N501 pin 5 TEMP relative to X503 pin 3 (=N501 pin 9) for ≅ 400...500 mV at about 20 °C. If not correct check the NTC in the battery pack for ≅12 kΩ at 20°C (X503 pins 3 and 5); check connections to N501.

3. N501 pin 6 (IMAXCHA) for ≅ 150 mV. If not correct check R514, and connections to N501.

4. N501 pin 7 (VBATHIGH) for ≅ 1.2V. If not correct check R513, and connections to N501.

Steps 1 to 4 verify that N501 supplies a 47 μA current to each of the resistors R512, battery NTC, R514, and R513

5. Check N501 pin 9 for the same voltage as on X503 pin 3 (sense resistors R504, R506, and R507).

6. If 1 to 5 above correct, then N501 is defective.

b. Connect TP531 for a short time (max. 1 minute) to ground, and see if the FET gate TP502 now shows a 100 kHz pulse signal.
If it does not, continue at step 7d.
If it does, the CHARCURR control signal is not correct, continue at step 7c.

c. Check the CHARCURR control signal:

The CHARCURR voltage on TP531 is controlled by a pulse width modulated voltage (CHARCUR) from the D-ASIC D471 (pin 40). The D-ASIC measures the required signals needed for control, via the Slow ADC.

1. Check the SLOW ADC, see Section 7.5.3.
2. Check VGARVAL (N501 pin 64), for +3.3V. If not correct, check if the line is shorted to ground. If it is not, then replace N501.
3. Trace the CHARCURR signal path to R534, R 442 and D471 (D-ASIC) output pin 40.

d. Check the following:

1. C506 and connections to N501.
2. Connections between V506 and N501 pin 16 (CHAGATE).
3. The voltage at TP501 (N501 pin 19, VCHDRIVE) for ≅ 15...20V.
4. The voltage at N501 pin 43 for a triangle waveform, 80...100 kHz, +1.6V to +3.2V.
5. If 1 to 4 correct, then replace N501.

7.4 Starting with a Dead Test Tool

If the test tool cannot be turned on, when powered by a charged battery pack, or by the power adapter, follow the steps below to locate the fault.

1. Connect a power adapter and a charged battery pack.
2. Turn the test tool on and listen if you hear a beep.
   a. If you hear no beep, continue at 7.4.1 Test Tool Completely Dead.
   b. If you hear a weak beep, continue at 7.4.2 Test Tool Software Does not Run.
   c. If you hear a “normal” beep, the software runs, but obviously the test tool is not operative. Continue at 7.4.3 Software Runs, Test Tool not Operative.

7.4.1 Test Tool Completely Dead

1. Turn the test tool off. Keep the keys  pressed, and turn the test tool on again.
   This will start up the mask software.
   If you still hear no beep, continue at step 2.
   If you hear a weak beep now, continue at Section 7.4.2.
2. Check the Keyboard ROW1 line (MS433 next to X452) for a 500 kHz 0.6V triangular wave. If not correct, continue at step 3.
   If correct, the mask software runs, but the buzzer circuit does not function. Check the buzzer function (Section 7.5.10), and then continue at Section 7.4.2.
3. Check N501 pin 60 (VBATSUP) for >4.8V. If not correct check R503, and connections to battery pack.
4. Check TP571 (+3V3GAR) for +3V3V.
   If not correct, this is possibly caused by V569, R580, TP571 short to ground, loose

pins of N501, or N501 defective. Check the +VD supply voltage on D-ASIC D471. Temporarily remove R470 to check for short circuit.

5. Check N501 pin 64 (VGARVAL) for +3.3V. If not correct:
   a. Check if the line is shorted to ground.
   b. Check N501 pin 73 (REFPWM2) for +3V3. REFPWM2 is supplied by N501, and derived from REFP on the reference circuit on the Trigger part. Check TP307 (N501 pin 72, REFP) for 1.22V, check V301/R307. If no 1.22V, and V301/R307 and connections are correct, then replace N501.
   c. Check N501 pin 12 (NETVALID) for +2.6V. If not correct, proceed as indicated in Section 7.3, step 6.
   d. Check the Power ON/OFF function, see Section 7.5.13.
6. Check X-tal signals on TP473 (32 kHz), TP474 (3.69 MHz), and TP475 (50 MHz); if not correct check connections, replace X-tals, replace D471. If the Test Tool is off AND not powered by the Battery Charger/Power Adapter, only the 32 kHz clock runs. If the 3.69 MHz clock is present, then continue at Section7.4.3.

7.4.2 Test Tool Software Does not Run.

1. Turn the test tool OFF and ON again.
2. Check D471 pin 59 (row1) for a 500 kHz triangular wave.
   If no 500 kHz is not present, but you hear a weak beep, the test tool software runs, but the buzzer circuit does not function correctly. Go to Section 7.5.10 to check the buzzer circuit, then continue at Section 7.4.3 to see why the test tool cannot be operated.
   If a 500 kHz triangular wave is present, the MASK software is running. Continue at step 3.
3. Load new software to see if the loaded software is corrupted. See Section 7.6.
4. Do the RAM test, see Section 7.5.12.
5. Check for bad soldered address/data lines and IC pins.
6. Replace FLASH-ROM D474 and RAM D475.

7.4.3 Software Runs, Test Tool not Operative

1. Check the Display and Backlight function, see Section 7.5.1
2. Check the Fly Back Converter, see Section 7.5.2
3. Check the Keyboard function, see Section 7.5.3

7.5 Miscellaneous Functions

7.5.1 Display and Back Light

Warning

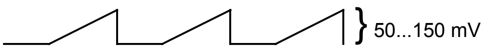
The voltage for the LCD back light fluorescent lamp is >400V!

1. Connect another LCD unit to see if the problem is caused by the LCD unit. The unit is not repairable.
2. Defective display
   Check the LCD control signals on measure spots MS401...MS422 (near to X453). Use a 10:1 probe with ground lead on the probe connected to the metal screening of the UUT. Notice that MS407 is missing !
   a. MS422: DISPON for +3.3V.
   b. MS420: DATACLK0 for 120 ns pulses
      MS414-415: LCDAT0,1 for 250 ns pulses
      MS417-418: LCDAT2,3 for 250 ns pulses
      MS412 LINECLK, for 120 ns pulses, ≅16 kHz
      MS411 FRAME, for 50 us pulses, ≅70 Hz
      MS409 M, for a ≅625Hz square wave.
   c. MS406 +5VA for +5V
      MS405 +3V3D for +3.3V
      MS401 -30VD for -30V (from Fly Back Converter).
   d. MS404 REFPWM1 for +3.3V.
3. Bad contrast.
   a. Check MS403 (CONTRAST) for a 60 kHz sinewave of 200 mVpp that rides on 0.8 Vdc.
   b. Check MS408 (LCDTEMP1) for +1.6V at room temperature (to SLOW ADC). If not correct, check R591 in SLOW ADC part.
4. Defective backlight:
   a. Turn the test tool on, and monitor the voltage on T600 pin 3 or pin 5 for a 8 Vpp, 66 kHz, half rectified sine wave. If a half rectified sine wave, with an increasing amplitude, is only seen for about 0.2 second directly after power on, then the secondary circuit is defective. Install a new LCD unit. If this does not cure the problem, check the resistance between T600 pin 10 and 6 for ≅300Ω, replace V603, V605. Check C606!
   b. Check T600 pin 3 and pin 5 for a 8 Vpp, 66 kHz, half rectified sine wave. If it is present on only pin 3 or pin 5, then replace V601.
   c. Check TP601 and TP602 for a 7Vpp, 66 kHz, square wave. If not correct then check TP604 (TLON) for +3V3. If TLON is correct, then replace N600.
   d. Check (replace) V600, V602.

5. Backlight brightness control not correct:
   Check the TP605 (BACKBRIG, supplied by D-ASIC D471) for a 25 kHz, 3.3 V pulse signal. The duty cycle of the pulses controls the back light brightness. The backlight brightness increases with an increasing length of the high pulse. Check V604, R604.
6. Measure the voltage on the collctro of V605:
   - correct voltage 1.5 V
   - >1.5 V : N600 defect
   - <1.5 V : secundary circuit defect (V606, V603, replace both if one is defective!)

7.5.2 Fly Back Converter

1. Check the voltages on TP572 (+5V), TP573 (+3.3V), TP574 (+3.3V), TP576 (-3.3V), TP577 (-30V) on the POWER part.
   a. If one or more voltages are correct, then check the rectifier diodes (V561...V564), and coils (L562...L567) of the incorrect voltage.
   b. If none of the voltages is correct, then the fly back converter does not run correctly, continue at step 2.
2. Check TP504 (VBATT) for >4.8V.
3. Check TP552 (FLYGATE) for a square wave voltage of at least some volts (for a correct Fly Back Converter 50...100 kHz, ≅10 Vpp).
   a. If a square wave is present on TP552 (may be not the correct value), then:
      1. Check the voltage on N501 pin 55 (FLYSENSP). For a correct converter this is a saw tooth voltage of 50...100 kHz, 50...150 mVpp).



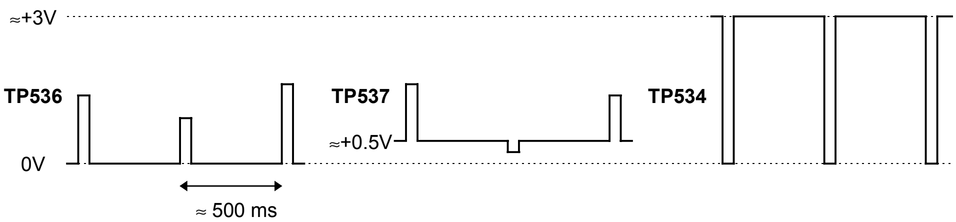
         a. If **no** sawtooth voltage is present on R501, no current, or a DC current flows in FET V554. The primary coil or V554 may be defective (or interrupted connections). Check R504, R506, R507 (battery current sense resistors); these resistors may be fused due to a short in FET V554.
         b. If an **incorrect** sawtooth is present on R501 this can be caused by:
            -overloaded outputs (Frequency low, e.g. <<50 kHz; 250 mVpp)
            -underloaded outputs (Frequency high, e.g. >>100 kHz; <<100 mVpp)
            -bad FET V554 (Sawtooth voltage is not linear).
      2. Check R570 and VCOIL connections.
   b. No FLYGATE square wave is present.
      Check TP526 (FREQPS) for a 50...100 kHz, 3.3 Vpp square wave. If no square wave on TP526, then go to step 4.
4. Check TP528 (PWRONOFF) for +3V. If not correct, see Section 7.5.13 Power ON/OFF.

5. Check N501 pin 43 (COSC) for a triangle waveform, 50...100 kHz, +1.6V to +3.2V. If not correct check C553 and connections; check IREF, see step 6. If all correct, replace N501.
6. Check N501 pin 74 (IREF) for 1.6V. If not correct:
   a. Check N501 pin 73 (REFPWM2) for +3V3. REFPWM2 is supplied by N501, and derived from REFP on the reference circuit on the Trigger part. Check TP307 (N501 pin 72, REFP) for 1.22V. If not correct, check V301/R307.
   b. Check R528, loose pin 74, or N501 defective.
7. Check N501 pin 51 (VOUTHI) for <2.5V (nominal value 1.65V). If not correct check R558 and connections to N501; check IREF, see step 6.
8. Check N501 pin 57 (IMAXFLY) for ≅250 mV. If not correct check R559 and connections to N501; check IREF, see step 6.

7.5.3 Slow ADC

Check the following signals:

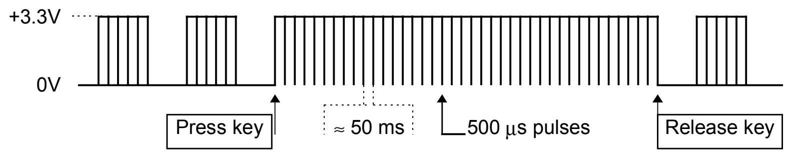
1. BATCUR (N501 pin 77), must be **{1.63+(6.7 x IBATP)}** Volt.
   If not correct, replace N501.
   Measure IBATP on X503 pin 3 (= N501 pin 9); IBATP senses the battery current.
2. BATVOLT (N501 pin 78), must be **{0.67 x (VBAT-3.27)}** Volt.
   If not correct, replace N501.
   Measure VBAT on TP504 (= N501 pin 3); VBAT senses battery the voltage.
3. BATTEMP (N501 pin 79), must be **{TEMP - IBATP}** Volt.
   If not correct, replace N501.
   Measure TEMP on N501 pin 5 (=X503 pin 6); TEMP senses the battery temperature.
   Measure IBATP on X503 pin 3 (= N501 pin 9); IBATP senses the battery current.
4. +3V3SADC must be +3.3V (supplied by N501 pin 65). If not correct, check if the +3V3SADC line is shorted to ground. If it is not, then replace N501.
5. SELMUXn (TP591, TP592, TP593) supplied by the D-ASIC must show LF pulses (0V to +3.3V, 0.5...3 seconds period).
6. Check TP536, TP537, and TP534 for signals shown below (typical examples, measured signals may have different pulse amplitude and repetition rate).
   TP536: if at a fixed level, replace D531.
   TP537: if not correct, trace signal to PWM circuit on the Digital part.
   TP534: if at a fixed level, replace N531.



7.5.4 Keyboard

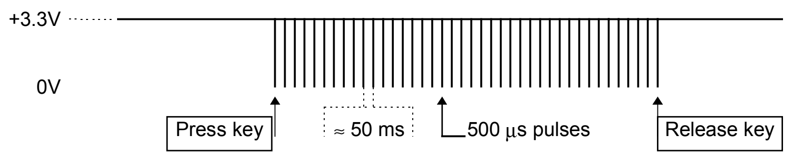
Proceed as follows if one or more keys cannot be operated.

1. Replace the key pad, and the key pad foil to see if this cures the problem.
2. Press a key, and check ROW0...5 (measure spots MS432..MS437) for the signal shown below :



If no key is pressed the ROW lines are low if a battery is installed; if the 123 is powered by the the mains adapter only, the lines are alternating pulsing and low.

3. Check COL0...3 (measure spots MS438...MS441) for a +3.3V level. Then press and hold a key, and check the matching COL line for the signal shown below:



If not correct, check the connections from X452 to D471; replace D471.

For the ON/OFF key see Section 7.5.13.

7.5.5 Optical Port (Serial RS232 Interface)

Receive (RXD)

1. Check the voltage RXDA on TP522 for +200 mV, and the voltage RXD on TP527 (buffered and amplified RXDA voltage) for +3.3V.
2. Shine with a lamp in the optical port (H522).
   Check the voltage RXDA on TP522 for 0...-0.6V, and the voltage RXD on TP527 for 0V. M

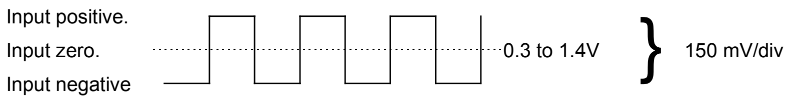
Send (TXD).

1. Check the voltage TXD on TP521 for +3.3V.
2. Press SAVE PRINT to open the **SAVE & PRINT** menu.
3. Press F2 **PRINT SCREEN** to start the test tool data output.
   Check the voltage TXD on TP521 for a burst of pulses (pulses from +2V to +3.3V).
   The length of the burst and the pulses depends on the selected baud rate.

7.5.6 Channel A, Channel B Voltage easurements

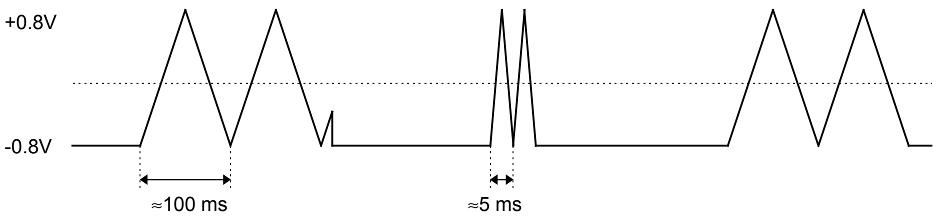
1. Press SCOPE MENU to open the **SCOPE INPUTS** menu, and select:
   INPUT A: ■ DC | ■ NORMAL | INPUT B: ■ DC | ■ NORMAL

2. Press SCOPE MENU to open the **SCOPE INPUTS** menu.
   Press F1 to open the **SCOPE OPTIONS ...** menu, and select:
   SCOPE MODE: ■ ROLL MODE | WAVEFORM MODE: ■ NORMAL.
3. Apply a 1 kHz square wave to Input A and Input B, and change the test tool sensitivity (V/div) to make the complete square wave visible.
4. Check TP154 (ADC-A) and TP254 (ADC-B) for the signal shown below:



   A trace amplitude of 1 division results in an 150 mV voltage on TP154/255
   Moving the trace position, with a zero input signal, results in a TP154/254 voltage of about +0.3V (bottom) to +1.4V (top).
   If the voltages are not correct, do steps 6 to 16; if these steps are correct, then replace the C-ASIC.
   If the voltages are correct, the error is most probably caused by the ADC, or ADC control: continue at step 16.
5. Check TP156 (TRIGA) and TP256 (TRIGB). The TRIGA and TRIGB signals must be the inverted input signals, with an amplitude of 50 mV per division trace amplitude.
   Moving the trace position, with a zero input signal, results in a TP156/256 voltage of about +0.4V (bottom) to -0.4V (top).
   If the voltages are not correct, do steps 6 to 16; if these steps are correct, then replace the C-ASIC.
6. Check the supply voltages +3V3A (+3.3V), -3V3A (-3.3V), and +5VA (+5V).
   If not correct trace to the Fly Back converter on the Power part.
7. Check TP151 (POS-A) and TP251 (POS-B) for about +1.1V (trace at mid-screen), +0.4V (trace at top of screen), +1.8V (trace at bottom of screen).
   If not correct check the PWM circuit (in the Digital Circuit).
8. Check TP152 (OFFSET-A) and TP252 (OFFSET-B) for about +1.1V.
9. Check TP303 (REFN) for -1.2V.
10. Check TP153 (DACTESTA) and TP253 (DACTESTB) for 0V. If TP153 is +1.7V, the C-ASIC is in the reset state (200 mV/div fixed sensitivity); check SDAT and SCLK, see step 15.
11. Check MIDADCA (N101/28) and TP255 MIDADCB (N201/28) for about +1.2V.
12. Press SCOPE MENU to open the **SCOPE INPUTS** menu.
    Press F1 to open the **SCOPE OPTIONS ...** menu, and select:
    SCOPE MODE: ■ NORMAL | WAVEFORM MODE: ■ NORMAL.
    Select a time base of 20 ms/div.

13. Check N101/31, N201/31 (TRACEROT supplied by T-ASIC N301) for the signals shown below (typical example at 20 ms/div.).



    If not correct check:
    TP432 (RAMPCLK) for 3V, 200 ns pulses.
    TP332 (RAMPCLK) for 0.6V, 200 ns pulses.
    TP331 (RSTRAMP) for +0.6V pulses, with varying pulse with and repetition rate.
    All pulses are supplied by D-ASIC-D471.

14. Check TP310 (REFATT) for alternating +1.2V and -1.2V pulses. The repetition frequency depends on the time base, and is for example 500 ms at 20 ms/div.
15. Check the SCLK and SDAT lines for +3.3V pulse bursts (C-ASIC pin 25 and 26). These signals can also be checked at TP471 (SCLK) and TP472 (SDAT).
16. Check SMPCLK_A (D401/15) and SMPCLK_B (D451/15) for a 5 MHz (time base ≥ 10 ms/div) or 25 MHz clock signal (3.3V). Check SMPCLK (N301/38) for a 5MHz or 25 MHz clock signal of 0.6V.
17. Check TP301 (REFADCT) for +2V, and TP302 (REFADCB) for +0.45V
18. Check the ADC supply voltages +3V3ADCA (D401/28, D451/28) and +3V3ADCD (D401/2, D451/2) for +3.3V.

7.5.7 Channel A Ohms and Capacitance Measurements

1. Press [VHzA Ω] and select **MEASURE on A: ■ OHMΩ.**
   Connect a current meter between Input A and the COM input. Select the various Ohms ranges, and verify that the current approximately matches the values listed in the table below.
   If not correct, the protection circuit or the current source in the T-ASIC (N301) may be defective.
   If the current is correct, and the Volt function is correct (so ADC is correct), then the Ohms part in the C-ASIC is defective: replace N101.

Range	50 Ω [1)]	500 Ω	5 kΩ	50 kΩ	500 kΩ	5 MΩ	30 MΩ
Current	500 μA	500 μA	50 μA	5 μA	0.5 μA	50 nA	50 nA

[1)] 50 Ω range for CONTINUITY only.

2. Press [VHzA Ω] and select **MEASURE on A: ■ CAP .**
   Verify TP156 for +0.3 ... 0V pulses (repetition rate 100...200 ms):
   Zero scale (open input): pulse width approximately 30 µs.
   Full scale (for example 500 nF): pulse width approximately 25 ms.
   If not correct, most probably the C-ASIC N101 is defective.
   If correct, continue at Section 7.5.8 Trigger functions (pulse width is measured via the T-ASIC).

7.5.8 Trigger Functions

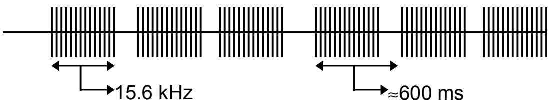
1. Press [VHzA Ω] and select **MEASURE on A: ■ VDC .**
2. Press [SCOPE MENU] and select **INPUT A: ■ DC | NORMAL | INPUT B: ■ DC | NORMAL**
3. Press [SCOPE MENU] to select the **SCOPE INPUTS** menu.
   Press [F3] to select the **TRIGGER** menu, and select:
   INPUT: ■ A or **B | SCREEN UPDATE: ■ FREE RUN | AUTO RANGE: . ■ >15HZ**

   Press [SCOPE MENU] to open the **SCOPE INPUTS** menu.
   Press [F1] to open the **SCOPE OPTIONS ...** menu, and select:
   SCOPE MODE: ■ NORMAL | WAVEFORM MODE: ■ NORMAL.
4. Supply a 1 kHz sine wave of +/- 3 divisions to Input A, and Input B.
5. Check:
   a. TP156, TP256 for a 600 mV (6 div. x 100 mV/div), 1 kHz, sine wave; the DC level depends on the trace position.
      If not correct, C-ASIC N101/N102 is probably defective.
   b. TP321, TP322 for 1.1...1.9V DC (move the trigger level from top to bottom).
      If not correct check the PWM circuit, see Section 7.5.8.
   c. TP311for a 0...+3.3V, 1 kHz square wave when the trigger level is at the middle of the trace). Change the trigger level, and verify that the duty cycle of the square wave changes. If not correct T-ASIC N301 may be defective.
   d. TP433 (TRIGDT) for 0...+3.3V pulses. Pulse width:
      4...10 µs for time base 2 µs/div and faster;
      >40 µs for time base 5 µs/div and slower; pulse width increases with time base.
   e. TP336 for +0.6...0V pulses, TP436 for +3.3...0V pulses; the pulse width is about 40 µs...10 ms.
      If not correct, check the RANDOMIZE circuit, see Section 7.5.15.
   f. SMPCLK_B (N301/38) for a 5 MHz (time base ≥ 10 ms/div) or 25 MHz (time base < 10 ms/div) clock signal (3.3V). Check SMPCLK_B on both sides of R339.
6. To test video trigger press [SCOPE MENU] to select the **SCOPE INPUTS** menu.

   Press [F3] to select the **TRIGGER** menu, and select **INPUT: ■ VIDEO on A...**
   From the **VIDEO TRIGGER** submenu select:
   SYSTEM: ■ PAL | LINE: ■ RANDOM | POLARITY: ■ POSITIVE
   Press [SCOPE MENU] to open the **SCOPE INPUTS** menu.

Press [F1] to open the **SCOPE OPTIONS ...** menu, and select:
SCOPE MODE: ■ NORMAL | WAVEFORM MODE: ■ NORMAL

7. Supply a 15.6 kHz square wave of 20V (+10...-10V) to Input A, and Input B.
8. Check:
   a. TP308 (TVOUT) for 15.6 kHz, -0.8...+0.6V pulse (square wave) bursts (see figure below).

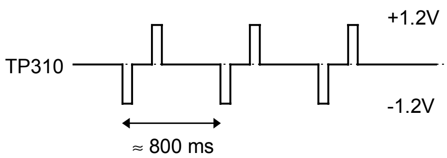


   If not correct, N301 may be defective.

   b. TVSYNC, on R392/R397, for 15.6 kHz, +2.6...+3.3V pulse bursts.
   If not correct, V395 may be defective.
   c. TP311 (ALLTRIG) for 15.6 kHz, +3.3...0V pulse bursts.
   If not correct, N301 may be defective.
   d. TP433 (TRIGDT) for 0...+3.3 pulses.
   If not correct, TRIGQUAL may be not correct.
   e. TP338 (TRIGQUAL) for 0...+0.6V pulses, width 70 µs, frequency about 2 kHz.
   If not correct, D471 may be defective.

7.5.9 Reference Voltages

1. Check:
   a. TP306 for +3.3V, TP307 for +1.23V
   If not correct check/replace V301, R307, C3112, P-ASIC N501.
   b. TP301 for +2V TP303 for -1.23V
   TP302 for +0.4V TP304 for +3.3V
   TP310, see figure below (in ROLL mode TP310 is zero).
   If not correct, check/replace REFERENCE GAIN circuit and T-ASIC N301.



7.5.10 Buzzer Circuit

1. Press [VHzA Ω] and select **MEASURE on A : CONT)))**
2. Short circuit Input A to COM. The buzzer is activated now.
3. Check TP496 for a 4 kHz, 0...3V square wave during beeping (0 V if not activated).
4. Check TP495 for a 4 kHz +3...-30V square wave during beeping (TP495 is -30V if the beeper is not activated).

7.5.11 Reset ROM Circuit

1. Check TP487 for +3V (supplied by D471).

7.5.12 RAM Test

You can use the Microsoft TERMINAL program to test the RAM. Proceed as follows:

1. Connect the Test Tool to a PC via the Optical Interface Cable PM9080.
2. Start the Terminal program, and select the following Settings:

Terminal Emulation	TTY (Generic)	
Terminal Preferences	Terminal Modes	CR -> CR/LF
	☒ Line Wrap	☒ Inbound
	☒ Local Echo	☐ Outbound
	☒ Sound	
Communications	Baud Rate	9600
	Data Bits	8
	Stop Bits	1
	Parity	None
	Flow Control	Xon/Xoff
	Connector	COMn

3. Turn the test tool off. Keep the keys  pressed, and turn the test tool on again. This will start up the mask software. You will hear a very weak beep now.
4. In the terminal program type capital characters X (no ENTER!). After a number of characters the test tool mask software will respond with an acknowledge 0 (zero). This indicates that the communication between the Terminal program and the test tool is accomplished.
5. Type `ID`
   and press [Enter]
   The test tool will return an acknowledge 0 (zero), and the string
   `Universal Host Mask software; UHM V3.0`
   If it does not, check the Terminal program settings, the interface connection, and the test tool Optical Port (Section 7.5.5).
6. Type `EX10,#H20400000,#H80000`
   and press [Enter]
   The test tool will return one of the following acknowledges:
   0 the RAM is OK.
   1 syntax error in the typed command
   6 the RAM does not properly function.

   Notice that the acknowledge overwites the first character of the message sent to the test tool.

7.5.13 Power ON/OFF

1. Check TP528 for +3V at power on, and 0V at power off (supplied by D471).
   If not correct, do the Section 7.4.1. tests first!

2. Check MS444 (ONKEY, D471) for +3V; when pressing the ON key the signal must be low for 100...150 ms.

7.5.14 PWM Circuit

1. Check the PWM control signals generated by D471. The signals must be measured on the small component (SMD) side of the Main PCA and must show 0...3V pulses, with variable duty cycle, and a frequency of 100, 25, or 6 kHz:
   a. CHARCURD (junction R442/C431) ≅ 100 kHz
   b. SADCLEV (R441/C432), POS A D (R439/C433), POS B D (R431/C442), TRIGLEV2D (R434/C438), TRIGLEV1D (R433/C439) ≅ 25 kHz
   c. OFFSETA-D (R438/C434), OFFSETB-D (R432/C441) ≅ 6 kHz
2. If not correct, check:
   a. TP306 (REFPWM2) for +3.3V (used for CHARCURD SADCLEV)
   b. TP304 (REFPWM1) for +3.3V (used for other PWM signals).

   If TP306 and TP304 are correct, D471 may be defective.

7.5.15 Randomize Circuit

1. Check TP483 for 0...+3V pulses, 25 kHz, variable duty cycle.
2. Check TP482, for +3...0V pulses, variable frequency and duty cycle.

7.6 Loading Software

To load instrument software in the test tool, the Fluke-43-123-19x ScopeMeter Loader program V3.0 is required.

Power the test tool via the power adapter input using the BC190 Power Adapter.

7.7 Configuration of CPLD-chip D470

The CPLD-chip (D470) must be programmed after being installed. CPLD is present on the Main PCA in the 123/124 ScopeMeter with installed software of version V2.00 and onwards (serial numbers approximately DM8250001 and onwards).
CPLD is a programmable device with solder connections of the Ball-Grid-Array (BGA) type. CPLD is supplied as a non-configured device. After the CPLD has been soldered on to the Main PCA, it must be configured.

To configure, the ScopeMeter Loader Program must be used and dedicated Loader and Model files. This has to be done in an Authorized Fluke Service Centre.

After configuring, it must be checked if if the CPLD-configuration was succesfull:

The function of CPLD is to assure that battery current drain is zero (<1 mA) after the ScopeMeter has been switched off. This current can be checked with a sensitive Digital Voltmeter across R504/R506/R507 (0.33 ohms). The check must be done 10 times after power off and every time current should not exceed 1 mA (with the mains adapter disconnected!).

A more direct check of correct CPLD-functioning is to check for a 61 us negative going pulse at test point TP480 at power off. TP480 carries CPLD output signal ‘enablemain’.

Chapter 8
List of Replaceable Parts

Title	Page

8.1 Introduction

This chapter contains an illustrated list of replaceable parts for the model 123 or 124 ScopeMeter test tool. Parts are listed by assembly; alphabetized by item number or reference designator. Each assembly is accompanied by an illustration showing the location of each part and its item number or reference designator. The parts list gives the following information:

- Item number or reference designator (for example, “R122”)
- An indication if the part is subject to static discharge: the * symbol
- Description
- Ordering code
- Location on the Main PCA (e.g. ‘C 4 Top’ or ‘B 3 Bottom’ on Top Side or Bottom Side of PCA).

Caution

A * symbol indicates a device that may be damaged by static discharge.

8.2 How to Obtain Parts

Contact an authorized Fluke service center.

To locate an authorized service center refer to the second page of this manual (back of the title page).

In the event that the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions, if necessary.

To ensure prompt delivery of the correct part, include the following information when you place an order:

- Instrument model (Fluke 123 or 124), 12 digit instrument code (9444 ... .), and serial number (DM.......). The items are printed on the type plate on the bottom cover.
- Ordering code
- Item number - Reference designator
- Description
- Quantity

8.3 Final Assembly Parts

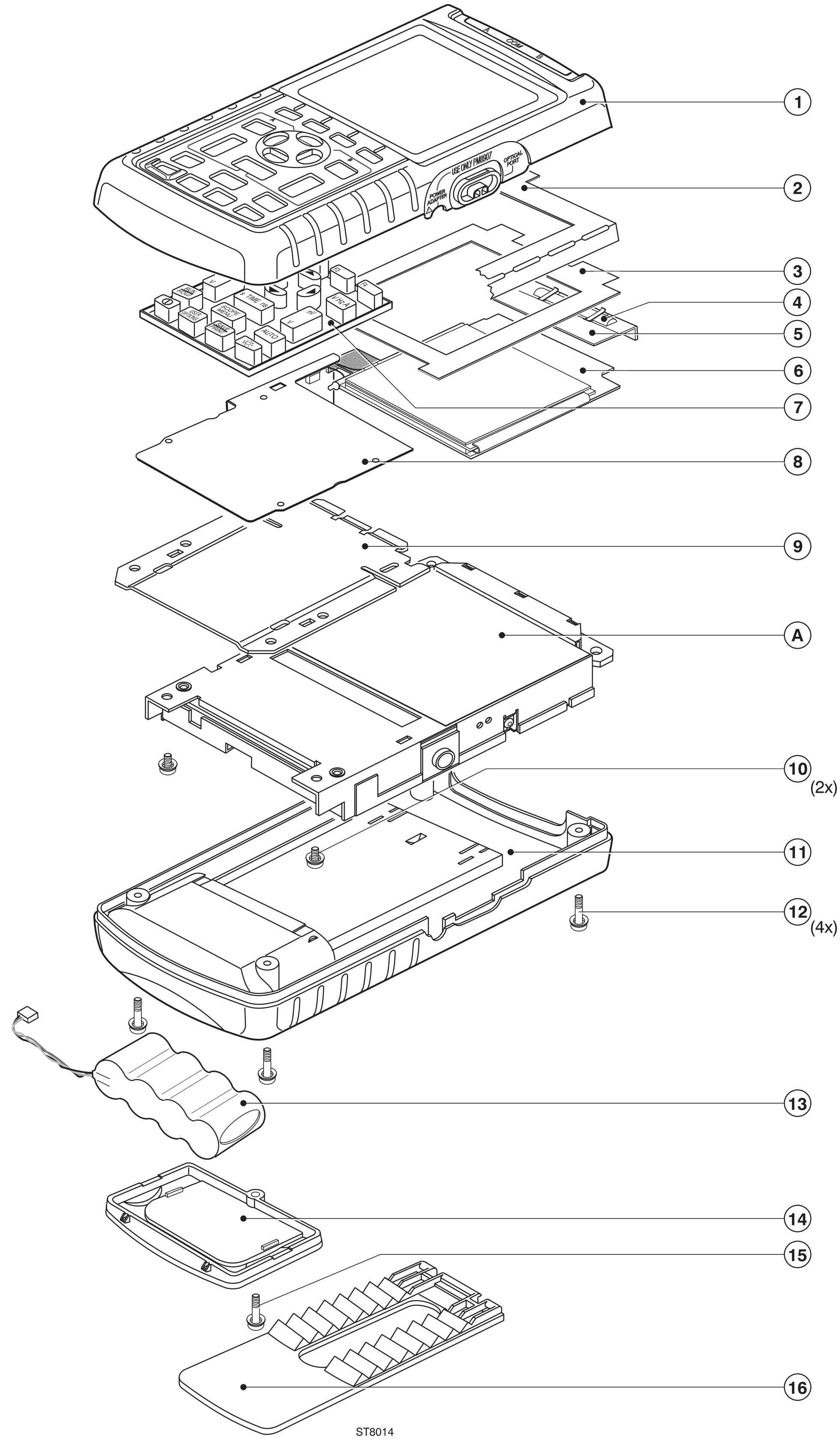
See Table 8-1 and Figure 8-1 for the Final Assembly parts.

Table 8-1. Final Assembly Parts

Item	Description	Ordering Code
1	top case assembly	5322 442 00272
1	window/decal (lens) Fluke 123	4022 240 12431
1	window/decal (lens) Fluke 124	4022 240 13031
2	shielding foil	5322 466 11434
3	dust seal	5322 466 11435
4	conductive foam strip	5322 466 11436
5	display shielding bracket	5322 402 10204
6	display assembly	5322 135 00029
7	keypad	5322 410 10397
8	keypad foil	5322 276 13711
9	keyboard pressure plate	5322 466 10963
10	combiscrew M3x10	5322 502 21507
11	bottom case	5322 442 00273
12	combiscrew M3x10	5322 502 21507
13a	battery pack (Ni-Cd as installed in Fluke 123)	BP120
13b	battery pack (Ni-MH as installed in Fluke 124)	BP130
14	battery door	4022 244 98491
15	combiscrew M3x10	5322 502 21507
16	bail	5322 466 10975
A	main PCA unit assembly. **No firmware loaded! Not calibrated**!	4022 246 19831

Note

The Test Tool contains a Rechargeable Ni-Cd (Model 123) or Ni-MH (Model 124) battery. Do not mix with the solid wastestream. Spent batteries should be disposed of by a qualified recycler or hazardous materials handler.



ST8014.EPS

Figure 8-1. Fluke 123/124 Final Assembly

8.4 Main PCA Unit Parts

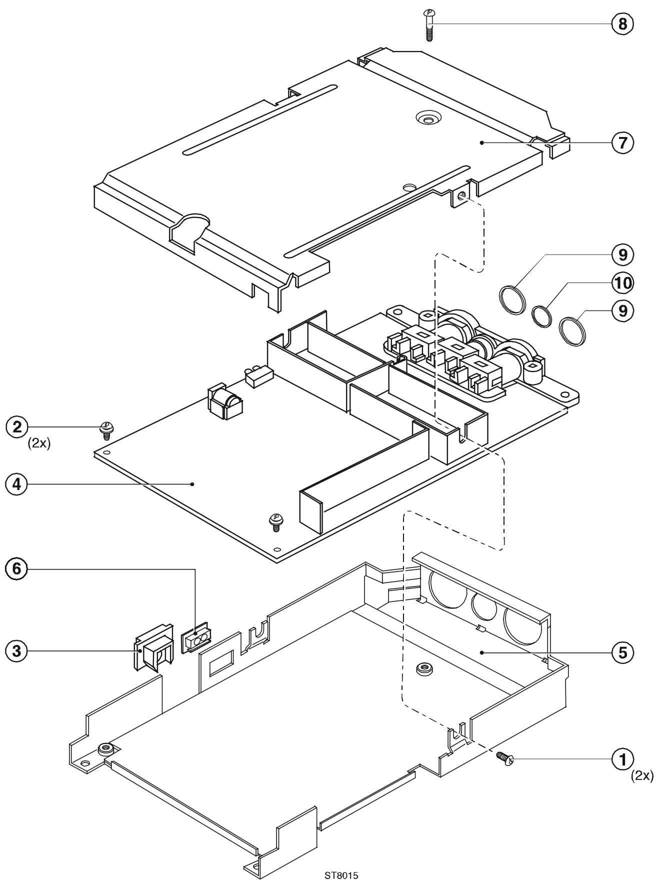
See Table 8-2 and Figure 8-2 for the Main PCA Unit parts.

Table 8-2. Main PCA Unit

Item	Description	Ordering Code
1	screw M2.5x5	5322 502 21206
2	combiscrew M3x10	5322 502 21507
3	insulator for power input	5322 325 10163
5	main PCA shielding box	5322 466 10976
6	guide piece for optical gate LEDs	5322 256 10201
7	main PCA shielding plate	5322 466 10964
8	screw M2.5x16	5322 502 14132
9	O-ring ∅ 17 mm Input A,B	5322 530 10272
10	O-ring ∅ 12 mm COM input	5322 530 10273

Note

If the main PCA must be replaced, you must order the complete Main PCA Unit.



ST8015.CGM

Figure 8-2. Main PCA Unit

8.5 Main PCA Parts

See Figure 9-6 and Figure 9-7 at the end of Chapter 9 for the Main PCA drawings.

Table 8-3. Main PCA

Reference Designator	Description	Ordering Code	PCA Location
1	Led Holder for H521 and H522	5322 255 41213	
2	Screw for Input Banana Jack Assembly	5322 502 14362	
3 (X100)	Input Banana Jack Assembly - without Input A,B and COM O-rings, see Figure 8-2. - including rersistors R1 and R2	5322 264 10311	
B401	QUARTZ CRYSTAL 32.768KHZ SEK	5322 242 10302	B5 Bottom
B402	QUARTZ CRYSTAL 3.6864MHZ KDK	4022 303 20201	C4 Top
B403	QUARTZ CRYSTAL 50MHZ KDK	4022 106 00021	C4 Top
C101	MKC FILM CAP 630V 10% 22NF	5322 121 10616	A 2 Top
C102	SUPPR CAPACIT0R 0.1 UF	5322 121 10527	A 1 Top
C104	CER.CAP. 3.15KV +-5% 120PF	5322 126 14046	B 2 Top
C105	ALCAP NICHICON 16V 10UF	5322 124 41979	B 3 Top
C106	CER.CAP. 1KV -20+80% 4.7NF	5322 126 13825	A 2 Top
C107	CER CHIP CAP 63V 5% 470PF	5322 122 32268	A 2 Bottom
C111	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	B 2 Top
C112	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	B 2 Top
C113	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	B 2 Top
C114	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	B 2 Top
C116	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	B 2 Top
C117	CER CAP 1 500V 2% 10PF	4822 122 31195	B 2 Top
C118	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	B 2 Top
C119	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	B 2 Top
C121	CER CAP 1 500V 2% 33PF	4822 122 31202	B 2 Top
C122	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	B 2 Top
C123	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	B 2 Top
C124	CER CAP 1 500V 2% 33PF	4822 122 31202	B 3 Top
C131	CER CHIP CAP 63V 0.25PF 0.82PF	5322 126 10786	A 2 Bottom

Reference Designator	Description	Ordering Code	PCA Location
C132	CER CHIP CAP 63V 0.25PF 4.7PF	5322 122 32287	A 2 Bottom
C133	CER CHIP CAP 63V 5% 47PF	5322 122 32452	A 2 Bottom
C134	CER CHIP CAP 63V 5% 470PF	5322 122 32268	A 2 Bottom
C136	CER CHIP CAP 63V 10% 4.7NF	5322 126 10223	A 2 Bottom
C142	CHIPCAP NP0 0805 5% 1NF	5322 126 10511	B 2 Bottom
C145	CHIPCAP NP0 0805 5% 1NF	5322 126 10511	A 2 Bottom
C146	CHIPCAP NP0 0805 5% 1NF	5322 126 10511	A 2 Top
C152	CERCAP X7R 0805 10% 15NF	4822 122 33128	A 2 Bottom
C153	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	A 2 Bottom
C156	CHIPCAP NP0 0805 5% 1NF	5322 126 10511	B 3 Bottom
C158	CER CHIP CAP 63V 5% 150PF	5322 122 33538	B 2 Bottom
C159	CHIPCAP NPO 0805 5% 100PF	5322 122 32531	B 2 Bottom
C161	CER CHIPCAP 25V 20% 100NF	5322 126 13638	A 2 Bottom
C181	ALCAP SANYO 10V 20% 22UF	5322 124 11837	A 3 Top
C182	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 2 Bottom
C183	ALCAP SANYO 10V 20% 22UF	5322 124 11837	B 3 Top
C184	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 2 Bottom
C186	CER CHIPCAP 25V 20% 100NF	5322 126 13638	A 2 Bottom
C187	ALCAP SANYO 10V 20% 22UF	5322 124 11837	B 3 Top
C188	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 2 Bottom
C189	CER CHIPCAP 25V 20% 100NF	5322 126 13638	A 2 Bottom
C190	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 2 Bottom
C191	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 2 Bottom
C199	CER CHIP CAP 63V 5% 470PF	5322 122 32268	A 3 Bottom
C201	MKC FILM CAP 630V 10% 22NF	5322 121 10616	C 2 Top
C202	SUPPR CAPACIT0R 0.1 UF	5322 121 10527	D 1 Top
C204	CER.CAP. 3.15KV +-5% 120PF	5322 126 14046	C 2 Top
C205	ALCAP NICHICON 16V 10UF	5322 124 41979	D 3 Top
C206	CER.CAP. 1KV -20+80% 4.7NF	5322 126 13825	D 1 Top
C207	CER CHIP CAP 63V 5% 470PF	5322 122 32268	C 2 Bottom
C211	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	D 2 Top

Reference Designator	Description	Ordering Code	PCA Location
C212	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	D 2 Top
C213	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	D 2 Top
C214	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	D 2 Top
C216	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	D 2 Top
C217	CER CAP 1 500V 2% 10PF	4822 122 31195	D 2 Top
C218	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	D 2 Top
C219	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	D 2 Top
C221	CER CAP 1 500V 2% 33PF	4822 122 31202	D 2 Top
C222	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	D 2 Top
C223	CER CAP 1 500V 0.25PF 4.7PF	5322 122 33082	D 2 Top
C224	CER CAP 1 500V 2% 33PF	4822 122 31202	D 3 Top
C231	CER CHIP CAP 63V 0.25PF 0.68PF	4822 126 12342	C 2 Bottom
C232	CER CHIP CAP 63V 0.25PF 4.7PF	5322 122 32287	C 2 Bottom
C233	CER CHIP CAP 63V 5% 47PF	5322 122 32452	C 2 Bottom
C234	CER CHIP CAP 63V 5% 470PF	5322 122 32268	C 2 Bottom
C236	CER CHIP CAP 63V 10% 4.7NF	5322 126 10223	C 2 Bottom
C242	CHIPCAP NP0 0805 5% 1NF	5322 126 10511	D 2 Bottom
C245	CHIPCAP NP0 0805 5% 1NF	5322 126 10511	C 2 Bottom
C246	CHIPCAP NP0 0805 5% 1NF	5322 126 10511	C 2 Top
C252	CERCAP X7R 0805 10% 15NF	4822 122 33128	C 2 Bottom
C253	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	C 2 Bottom
C256	CHIPCAP NP0 0805 5% 1NF	5322 126 10511	D 3 Bottom
C258	CER CHIP CAP 63V 5% 150PF	5322 122 33538	C 2 Bottom
C259	CHIPCAP NPO 0805 5% 100PF	5322 122 32531	C 2 Bottom
C261	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 2 Bottom
C281	ALCAP SANYO 10V 20% 22UF	5322 124 11837	C 3 Top
C282	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 2 Bottom
C283	ALCAP SANYO 10V 20% 22UF	5322 124 11837	C 3 Top
C284	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 2 Bottom
C286	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 2 Bottom
C287	ALCAP SANYO 10V 20% 22UF	5322 124 11837	D 3 Top
C288	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 2 Bottom

Reference Designator	Description	Ordering Code	PCA Location
C289	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 2 Bottom
C290	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 2 Bottom
C291	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 2 Bottom
C301	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 3 Bottom
C303	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 3 Top
C306	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 3 Bottom
C311	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 3 Bottom
C312	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 3 Bottom
C313	ALCAP SANYO 25V 20% 10UF	5322 124 11838	D 3 Top
C314	ALCAP SANYO 25V 20% 10UF	5322 124 11838	A 3 Top
C317	ALCAP NICHICON 6.3V 20% 22UF	4822 124 80675	C 3 Top
C321	CER CHIP CAP 63V 10% 1.5NF	5322 122 31865	C 3 Top
C322	CER CHIP CAP 63V 10% 1.5NF	5322 122 31865	C 3 Top
C331	CER CHIP CAP 63V 0.25PF 4.7PF	5322 122 32287	B 3 Bottom
C332	CER CHIP CAP 63V 5% 22PF	5322 122 32658	B 4 Bottom
C333	CER CHIP CAP 63V 0.25PF 1PF	5322 122 32447	B 3 Top
C337	CER CHIP CAP 63V 0.25PF 4.7PF	5322 122 32287	B 3 Top
C339	CER CHIP CAP 63V 0.25PF 1PF	5322 122 32447	B 3 Top
C342	CER CHIP CAP 63V 0.25PF 1PF	5322 122 32447	B 3 Bottom
C344	CER CHIP CAP 63V 5% 22PF	5322 122 32658	B 3 Bottom
C356	CER CHIP CAP 63V 10% 18NF	5322 126 14044	B 3 Bottom
C357	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	B 3 Bottom
C376	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 3 Bottom
C377	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 3 Bottom
C378	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 3 Bottom
C379	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 3 Bottom
C381	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 3 Bottom
C382	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 3 Bottom
C391	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 3 Bottom
C392	ALCAP NICHICON 16V 10UF	5322 124 41979	D 3 Top
C393	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 3 Bottom
C394	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 3 Bottom
C395	CER CHIP CAP 25V 20% 47NF	5322 126 14045	C 3 Top

Reference Designator	Description	Ordering Code	PCA Location
C396	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 3 Bottom
C397	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 3 Bottom
C398	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 3 Bottom
C399	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 3 Top
C400	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	A 5 Top
C401	CER CHIP CAP 63V 0.25PF 4.7PF	5322 122 32287	B 3 Bottom
C402	CER CHIPCAP 16V 10% 100NF	4022 301 61681	B 3 Bottom
C403	CER CHIPCAP 16V 10% 100NF	4022 301 61681	B 3 Bottom
C404	CER CHIP CAP 63V 5% 470PF	5322 122 32268	A 4 Bottom
C405	CER CHIPCAP 16V 10% 100NF	4022 301 61681	B 3 Bottom
C406	ALCAP 6.3V 10UF	4022 101 00011	B 3 Bottom
C407	CER CHIPCAP 16V 10% 100NF	4022 301 61681	B 3 Bottom
C408	CER CHIPCAP 16V 10% 100NF	4022 301 61681	B 3 Bottom
C409	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	A 3 Bottom
C410	CER CHIPCAP 16V 10% 100NF	4022 301 61681	B 3 Bottom
C415	ALCAP 6.3V 10UF	4022 101 00011	C 3 Top
C416	CER CHIPCAP 16V 10% 100NF	4022 301 61681	B 3 Bottom
C431	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 4 Bottom
C432	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 4 Bottom
C433	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	B 4 Bottom
C434	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	C 3 Bottom
C436	CER CAP X5R 1206 10% 1UF	5322 126 14089	B 4 Bottom
C438	CER CHIP CAP 63V 10% 4.7NF	5322 126 10223	C 4 Bottom
C439	CER CHIP CAP 63V 10% 4.7NF	5322 126 10223	C 4 Bottom
C441	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	B 4 Bottom
C442	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	B 4 Bottom
C451	CER CHIP CAP 63V 0.25PF 4.7PF	5322 122 32287	C 3 Bottom
C452	CER CHIPCAP 16V 10% 100NF	4022 301 61681	C 3 Bottom
C453	CER CHIPCAP 16V 10% 100NF	4022 301 61681	C 3 Bottom
C455	CER CHIPCAP 16V 10% 100NF	4022 301 61681	C 3 Bottom
C456	ALCAP 6.3V 10UF	4022 101 00011	C 3 Bottom
C457	CER CHIPCAP 16V 10% 100NF	4022 301 61681	C 3 Bottom
C458	CER CHIPCAP 16V 10% 100NF	4022 301 61681	C 3 Bottom
C460	CER CHIPCAP 16V 10% 100NF	4022 301 61681	C 3 Bottom

Reference Designator	Description	Ordering Code	PCA Location
C463	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 4 Bottom
C464	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 4 Bottom
C465	ALCAP 6.3V 10UF	4022 101 00011	D 3 Top
C466	CER CHIPCAP 16V 10% 100NF	4022 301 61681	C 3 Bottom
C470	CER CHIPCAP 50V 10% 100NF	4022 301 61331	B 4 Bottom
C471	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 4 Bottom
C472	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 4 Bottom
C473	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 4 Bottom
C474	CER CHIPCAP 25V 20% 100NF	5322 126 13638	A 4 Bottom
C475	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 5 Bottom
C477	CER CHIPCAP 50V 10% 100NF	4022 301 61331	A 4 Bottom
C478	CER CHIPCAP 25V 20% 100NF	5322 126 13638	A 4 Bottom
C479	CER CHIP CAP 63V 5% 22PF	5322 122 32658	B 4 Bottom
C480	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 4 Bottom
C481	CER CHIP CAP 50V 5% 18PF	4022 301 60201	C 4 Bottom
C482	CER CHIP CAP 50V 5% 18PF	4022 301 60201	C 4 Bottom
C483	CER CHIP CAP 50V 5% 18PF	4022 301 60201	C 4 Bottom
C484	CER CHIP CAP 50V 5% 18PF	4022 301 60201	C 4 Bottom
C485	CER CHIP CAP 50V 6% 4.7PF	4022 301 60131	B 4 Bottom
C487	CHIPCAP NPO 0805 5% 100PF	5322 122 32531	C 3 Bottom
C488	CHIPCAP NPO 0805 5% 100PF	5322 122 32531	C 3 Bottom
C489	CC 22NF 10% 0805 X7R 50 V	4022 301 60491	C 4 Bottom
C490	CER CHIP CAP 50V 5% 180PF	4022 301 60321	C 4 Bottom
C491	CER CHIPCAP 50V 10% 100NF	4022 301 61331	B 5 Top
C492	CER CHIPCAP 50V 10% 100NF	4022 301 61331	C 4 Bottom
C493	CER CHIPCAP 50V 10% 100NF	4022 301 61331	B 4 Bottom
C500	1UF CERCAP Y5V 1206 10%	5322 126 14086	D 3 Top
C501	ELCAP 25V 20% 180UF	5322 124 11843	D 3 Top
C502	ALCAP NICHICON 25V 20% 10UF	5322 124 11839	C 4 Top
C503	ELCAP 10V 20% 390UF	5322 124 11844	D 4 Top
C504	ALCAP NICHICON 16V 10UF	5322 124 41979	C 4 Top
C505	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 4 Bottom
C506	CER CHIP CAP 25V 20% 47NF	5322 126 14045	D 5 Bottom
C507	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 5 Bottom

Reference Designator	Description	Ordering Code	PCA Location
C509	CER CAP X5R 1206 10% 1UF	5322 126 14089	D 5 Bottom
C511	CER CHIPCAP 25V 20% 100NF	5322 126 13638	A 5 Bottom
C512	CER CHIPCAP 25V 20% 100NF	5322 126 13638	A 5 Bottom
C528	ALCAP NICHICON 6.3V 20% 22UF	4822 124 80675	D 4 Top
C529	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 4 Bottom
C531	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	C 4 Bottom
C532	CC 22NF 10% 0805 X7R 50V	4022 301 60491	C 4 Bottom
C533	CER CHIPCAP 50V 10% 22NF	4022 301 60491	C 4 Bottom
C534	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 4 Bottom
C547	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	D 5 Bottom
C548	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	D 5 Bottom
C549	CHIPCAP X7B 0805 10% 22NF	5322 122 32654	D 4 Bottom
C550	CER CHIP CAP 63V 10% 4.7NF	5322 126 10223	D 5 Bottom
C551	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 5 Bottom
C552	CER CHIPCAP 25V 20% 100NF	5322 126 13638	D 5 Bottom
C553	CER CHIP CAP 63V 5% 150PF	5322 122 33538	C 5 Top
C554	CER CAP X5R 1206 10% 1UF	5322 126 14089	A 5 Bottom
C555	ELCAP 10V 20% 390UF	5322 124 11844	C 5 Top
C561	ALCAP SANYO 6,3V 20% 150UF	5322 124 11841	C 5 Top
C562	ALCAP SANYO 6,3V 20% 150UF	5322 124 11841	B 5 Top
C563	ALCAP SANYO 6,3V 20% 150UF	5322 124 11841	B 5 Top
C564	ALCAP SANYO 35V 20% 47UF	5322 124 11842	A 5 Top
C565	ALCAP SANYO 6,3V 20% 150UF	5322 124 11841	B 5 Top
C567	ALCAP SANYO 6,3V 20% 150UF	5322 124 11841	B 5 Top
C568	ALCAP SANYO 6,3V 20% 150UF	5322 124 11841	D 5 Top
C572	ALCAP SANYO 6,3V 20% 150UF	5322 124 11841	C 5 Top
C573	ALCAP SANYO 6,3V 20% 150UF	5322 124 11841	B 5 Top
C574	ALCAP SANYO 6,3V 20% 150UF	5322 124 11841	A 5 Top
C576	ALCAP SANYO 6,3V 20% 150UF	5322 124 11841	B 5 Top
C583	CER CHIPCAP 50V 10% 100NF	4022 301 61331	C583 D 4 Bottom
C591	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C591 C 5 Bottom
C592	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 5 Bottom
C593	CER CHIPCAP 25V 20% 100NF	5322 126 13638	C 5 Bottom
C594	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 5 Bottom

Reference Designator	Description	Ordering Code	PCA Location
C602	CER CHIP CAP 25V 20% 47NF	5322 126 14045	A 5 Bottom
C603	CER CHIPCAP 25V 20% 100NF	5322 126 13638	A 4 Bottom
C604	CER CAP X5R 1206 10% 1UF	5322 126 14089	A 5 Bottom
C605	CHIPCAP NP0 0805 5% 1NF	5322 126 10511	A 5 Bottom
C606	CER CHIPCAP 25V 20% 100NF	5322 126 13638	B 5 Bottom
C607	CHIPCAP X7R 0805 10% 10NF	5322 122 34098	B 5 Bottom
C608	MKT FILM CAP 63V 10% 100NF	5322 121 42386	B 5 Top
C609	CER.CAP. 2KV +-5% 33PF	5322 126 14047	A 4 Top
C610	CER CAP X5R 1206 10% 1UF	5322 126 14089	B 5 Bottom
C611	CER CHIPCAP 50V 5% 1NF	4022 301 60411	B 5 Top
D401 *	AD-CONV AD9280ARSRL	4022 103 00121	B 3 Top
D451 *	AD-CONV AD9280ARSRL	4022 103 00121	C 3 Top
D470 *	CPLD XCR3032XL-5CS48C	4022 103 00111	C 4 Top
D471 *	D-ASIC SPIDER	4022 304 11551	B 4 Top
D472 *	NC7WZ17-UHS	4022 304 11691	C 5 Top
D473 *	TPS3823-25DBVR	4022 304 11701	B 4 Bottom
D474 *	16M FEPROM SST39VF800A-90-4C-EK	4022 103 01751	A 4 Top
D475 *	SRAM CY62146VLL-70BAI	4022 304 11361	B 5 Top
D531 *	8-INP MUX 74HC4051D PEL	5322 209 61483	C 4 Bottom
H495	PE BUZZER PKM13EPP-4002 MUR	5322 280 10311	A 3 Top
H521	IR LED OP266A	4022 103 01021	D 3 Top
H522	PHOTODIODE OP906 OPT	5322 130 10777	D 3 Top
K171	DPDT RELAY ASL-1.5W-K-B05	5322 280 10309	A 2 Top
K173	DPDT RELAY DSP1-L-1,5V MAT	5322 280 10312	A 2 Top
K271	DPDT RELAY ASL-1.5W-K-B05	5322 280 10309	C 2 Top

Reference Designator	Description	Ordering Code	PCA Location
L181	CHIP INDUCT. 47UH 10% TDK	4822 157 70794	B 3 Bottom
L182	CHIP INDUCT. 47UH 10% TDK	4822 157 70794	A 3 Bottom
L183	CHIP INDUCT. 47UH 10% TDK	4822 157 70794	A 3 Bottom
L281	CHIP INDUCT. 47UH 10% TDK	4822 157 70794	D 3 Bottom
L282	CHIP INDUCT. 47UH 10% TDK	4822 157 70794	C 3 Bottom
L283	CHIP INDUCT. 47UH 10% TDK	4822 157 70794	C 3 Bottom
L421	FILTER T 25MHZ MEM2012T25R0	4022 104 00321	A 4 Top
L422	FILTER T 25MHZ MEM2012T25R0	4022 104 00321	A 4 Top
L423	FILTER T 25MHZ MEM2012T25R0	4022 104 00321	A 4 Top
L424	FILTER T 25MHZ MEM2012T25R0	4022 104 00321	A 3 Top
L425	FILTER T 25MHZ MEM2012T25R0	4022 104 00321	A 3 Top
L426	FILTER T 25MHZ MEM2012T25R0	4022 104 00321	A 4 Top
L427	FILTER T 25MHZ MEM2012T25R0	4022 104 00321	A 3 Top
L428	FILTER T 25MHZ MEM2012T25R0	4022 104 00321	A 4 Top
L480	CHIP INDUCT. 1UH 5% TDK	5322 157 63648	C 4 Bottom
L501	CHOKE 33UH TDK	5322 157 10994	D 4 Top
L502	FILTER EMI 330E 0805 MUR	4022 104 00311	A 5 Bottom
L503	FILTER EMI 330E 0805 MUR	4022 104 00311	A 5 Top
L504	FILTER EMI 330E 0805 MUR	4022 104 00311	A 5 Bottom
L505	FILTER EMI 330E 0805 MUR	4022 104 00311	A 5 Bottom
L506	FILTER EMI 330E 0805 MUR	4022 104 00311	D 4 Bottom
L507	FILTER EMI 330E 0805 MUR	4022 104 00311	D 4 Bottom
L562	CHIP INDUCT. 47UH 10% TDK	4822 157 70794	B 5 Bottom
L563	CHIP INDUCT. 47UH 10% TDK	4822 157 70794	B 5 Bottom
L564	FIXED INDUCOR 68UH 10% TDK	5322 157 10995	A 5 Top
L566	FIXED INDUCOR 68UH 10% TDK	5322 157 10995	B 5 Top
L567	CHIP INDUCT. 47UH 10% TDK	4822 157 70794	B 5 Bottom
L569	FIXED INDUCOR 68UH 10% TDK	5322 157 10995	D 5 Top
L600	SHIELDED CHOKE 150UH TDK	5322 157 10996	A 5 Top
N101 *	C-ASIC OQ0258	5322 209 13141	B 2 Top
N201 *	C-ASIC OQ0258	5322 209 13141	C 2 Top
N301 *	T-ASIC OQ0257	5322 209 13142	B 3 Top

Reference Designator	Description	Ordering Code	PCA Location
N501 *	P-ASIC OQ0256	5322 209 13143	D 5 Top
N532 *	LOW POW OPAMP LMC7101BIM5X NSC	5322 209 15144	C 4 Bottom
N534 *	LOW POW OPAMP LMC7101BIM5X NSC	5322 209 15144	C 4 Bottom
N531 *	LOW POW OPAMP LMC7101BIM5X NSC	5322 209 15144	
N534 *	OPAMP LMC7101BIM5X	5322 209 15144	C 4 Bottom
N600 *	LAMP CONTROLLER UC3872DW UNI	5322 209 14851	A 5 Bottom
R1	MTL FILM RST VR25 5% 220K 0,25W	4822 053 20224	B 1 Top
R2	MTL FILM RST VR25 5% 220K 0,25W	4822 053 20224	C 1 Top
R101	MTL FILM RST MRS25 1% 487K	4822 050 24874	B 2 Top
R102	MTL FILM RST MRS25 1% 487K	4822 050 24874	B 2 Top
R103	RESISTOR CHIP TC50 1% 1M	4022 301 22441	A 2 Top
R104	RESISTOR CHIP RC12H 1% 26K1	5322 117 12448	A 2 Top
R105	RESISTOR CHIP TC100 1% 147E	4022 301 21631	B 2 Top
R106	PTC THERM DISC 600V 300-500E	5322 116 40274	A 1 Top
R108	RESISTOR CHIP RC11 2A 0E	4022 301 21281	B 2 Top
R109	RESISTOR CHIP RC12H 1% 2K15	5322 117 12452	A 2 Bottom
R110	RESISTOR CHIP RC12H 1% 2K15	5322 117 12452	B 2 Bottom
R111	RESISTOR CHIP RC11 2% 10M	4822 051 20106	B 2 Bottom
R112	RESISTOR CHIP RC11 2% 10M	4822 051 20106	B 2 Bottom
R113	RESISTOR CHIP RC11 2% 10M	4822 051 20106	B 2 Bottom
R114	RESISTOR CHIP RC11 2% 10M	4822 051 20106	B 2 Bottom
R116	RESISTOR CHIP RC12H 1% 215E	5322 117 12453	B 2 Bottom
R117	RESISTOR CHIP RC12H 1% 215E	5322 117 12453	B 2 Bottom
R118	RESISTOR CHIP RC12H 1% 68E1	5322 117 12454	B 2 Bottom
R119	RESISTOR CHIP RC12H 1% 464E	5322 117 12455	B 3 Bottom
R120	RESISTOR CHIP RC11 2% 10M	4822 051 20106	B 2 Bottom
R121	RESISTOR CHIP RC12H 1% 68E1	5322 117 12454	B 2 Bottom
R125	RESISTOR CHIP RC12H 1% 68E1	5322 117 12454	B 2 Bottom
R131	RESISTOR CHIP RC12G 1% 1M	5322 117 12484	A 2 Bottom
R132	RESISTOR CHIP RC12G 1% 100K	5322 117 12485	A 2 Bottom

Reference Designator	Description	Ordering Code	PCA Location
R133	RESISTOR CHIP RC12G 1% 10K	5322 117 12486	A 2 Bottom
R134	RESISTOR CHIP RC12G 1% 1K	5322 117 12487	A 2 Bottom
R136	RESISTOR CHIP RC-02G 1% 100E	4822 051 51001	A 2 Bottom
R137	RESISTOR CHIP RC-02H 1% 56K2	5322 117 10574	A 1 Bottom
R138	RESISTOR CHIP RC-02H 1% 56K2	5322 117 10574	A 1 Bottom
R139	RESISTOR CHIP RC-02H 1% 56K2	5322 117 10574	A 1 Bottom
R140	RESISTOR CHIP RC-02H 1% 56K2	5322 117 10574	A 1 Bottom
R141	RESISTOR CHIP RC12G 1% 215K	5322 117 12488	B 2 Bottom
R142	RESISTOR CHIP RC12G 1% 147K	5322 117 12489	A 2 Bottom
R143	RESISTOR CHIP RC12G 1% 909K	5322 117 12491	A 2 Bottom
R144	RESISTOR CHIP RC12H 1% 348E	5322 117 12456	A 2 Bottom
R146	RESISTOR CHIP RC12H 1% 215K	5322 117 12457	A 2 Bottom
R151	RESISTOR CHIP TC50 1% 100K	4022 301 22311	A 2 Bottom
R152	RESISTOR CHIP TC50 1% 100K	4022 301 22311	A 2 Bottom
R153	RESISTOR CHIP RC12H 1% 681K	5322 117 12485	A 2 Bottom
R154	RESISTOR CHIP RC12H 1% 681K	5322 117 12458	A 2 Bottom
R155	RESISTOR CHIP RC12H 1% 178K	5322 117 12459	A 2 Bottom
R156	RESISTOR CHIP TC50 1% 100K	4022 301 22311	B 3 Bottom
R157	RESISTOR CHIP TC100 1% 162E	4022 301 21641	B 3 Bottom
R158	RESISTOR CHIP RC11 2A 0E	4022 301 21281	B 3 Bottom
R159	RESISTOR CHIP RC12H 1% 100E	4822 117 11373	A 3 Bottom
R160	RESISTOR CHIP RC12H 1% 51K1	5322 117 12462	B 2 Bottom
R161	RESISTOR CHIP TC50 1% 100K	4022 301 22311	B 3 Bottom
R165	RESISTOR CHIP RC12H 1% 100E	4822 117 11373	A 3 Bottom
R171	RESISTOR CHIP RC12H 1% 348E	5322 117 12456	A 3 Bottom
R172	PTC THERM DISC 600V 300-500E	5322 116 40274	A 2 Top
R173	RESISTOR CHIP RC12H 1% 348E	5322 117 12456	A 3 Bottom
R182	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	B 3 Bottom
R184	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	B 2 Bottom
R186	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	A 2 Bottom
R188	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	B 3 Bottom
R189	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	A 2 Bottom
R201	MTL FILM RST MRS25 1% 487K	4822 050 24874	C 2 Top

Reference Designator	Description	Ordering Code	PCA Location
R202	MTL FILM RST MRS25 1% 487K	4822 050 24874	C 2 Top
R203	RESISTOR CHIP TC50 1% 1M	4022 301 22441	C 2 Top
R204	RESISTOR CHIP RC12H 1% 26K1	5322 117 12448	C 2 Top
R205	RESISTOR CHIP TC100 1% 147E	4022 301 21631	D 2 Top
R206	PTC THERM DISC 600V 300-500E	5322 116 40274	D 1 Top
R208	RESISTOR CHIP RC11 2A 0E	4022 301 21281	D 2 Top
R209	RESISTOR CHIP RC12H 1% 2K15	5322 117 12452	C 2 Bottom
R210	RESISTOR CHIP RC12H 1% 2K15	5322 117 12452	D 2 Bottom
R211	RESISTOR CHIP RC11 2% 10M	4822 051 20106	D 2 Bottom
R212	RESISTOR CHIP RC11 2% 10M	4822 051 20106	D 2 Bottom
R213	RESISTOR CHIP RC11 2% 10M	4822 051 20106	D 2 Bottom
R214	RESISTOR CHIP RC11 2% 10M	4822 051 20106	D 2 Bottom
R216	RESISTOR CHIP RC12H 1% 215E	5322 117 12453	D 2 Bottom
R217	RESISTOR CHIP RC12H 1% 215E	5322 117 12453	D 2 Bottom
R218	RESISTOR CHIP RC12H 1% 68E1	5322 117 12454	D 2 Bottom
R219	RESISTOR CHIP RC12H 1% 464E	5322 117 12455	D 3 Bottom
R220	RESISTOR CHIP RC11 2% 10M	4822 051 20106	D 2 Bottom
R221	RESISTOR CHIP RC12H 1% 68E1	5322 117 12454	D 2 Bottom
R225	RESISTOR CHIP RC12H 1% 68E1	5322 117 12454	D 2 Bottom
R231	RESISTOR CHIP RC12G 1% 1M	5322 117 12484	C 2 Bottom
R232	RESISTOR CHIP RC12G 1% 100K	5322 117 12485	C 2 Bottom
R233	RESISTOR CHIP RC12G 1% 10K	5322 117 12486	C 2 Bottom
R234	RESISTOR CHIP RC12G 1% 1K	5322 117 12487	C 2 Bottom
R236	RESISTOR CHIP RC-02G 1% 100E	4822 051 51001	C 2 Bottom
R237	RESISTOR CHIP RC-02H 1% 56K2	5322 117 10574	D 1 Bottom
R238	RESISTOR CHIP RC-02H 1% 56K2	5322 117 10574	D 1 Bottom
R239	RESISTOR CHIP RC-02H 1% 56K2	5322 117 10574	D 1 Bottom
R240	RESISTOR CHIP RC-02H 1% 56K2	5322 117 10574	D 1 Bottom
R241	RESISTOR CHIP RC12G 1% 215K	5322 117 12488	D 2 Bottom
R242	RESISTOR CHIP RC12G 1% 147K	5322 117 12489	C 2 Bottom
R243	RESISTOR CHIP RC12G 1% 909K	5322 117 12491	C 2 Bottom
R246	RESISTOR CHIP RC12H 1% 215K	5322 117 12457	C 2 Bottom
R251	RESISTOR CHIP TC50 1% 100K	4022 301 22311	C 2 Bottom

Reference Designator	Description	Ordering Code	PCA Location
R252	RESISTOR CHIP TC50 1% 100K	4022 301 22311	C 2 Bottom
R253	RESISTOR CHIP RC12H 1% 681K	5322 117 12458	C 2 Bottom
R254	RESISTOR CHIP RC12H 1% 681K	5322 117 12458	C 2 Bottom
R255	RESISTOR CHIP RC12H 1% 178K	5322 117 12459	C 2 Bottom
R256	RESISTOR CHIP TC50 1% 100K	4022 301 22311	D 3 Bottom
R257	RESISTOR CHIP TC100 1% 133E	4022 301 21621	D 3 Bottom
R258	RESISTOR CHIP RC11 2A 0E	4022 301 21281	C 3 Bottom
R259	RESISTOR CHIP RC12H 1% 100E	4822 117 11373	C 3 Bottom
R260	RESISTOR CHIP RC12H 1% 51K1	5322 117 12462	D 2 Bottom
R261	RESISTOR CHIP TC50 1% 100K	4022 301 22311	D 3 Bottom
R271	RESISTOR CHIP RC12H 1% 348E	5322 117 12456	C 3 Bottom
R282	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	D 3 Bottom
R284	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	D 2 Bottom
R286	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	C 3 Bottom
R288	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	D 3 Bottom
R289	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	C 2 Bottom
R301	RESISTOR CHIP TC100 1% 5K62	4022 301 22011	B 3 Bottom
R302	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 3 Bottom
R303	RESISTOR CHIP TC100 1% 34K8	4022 301 22201	B 3 Bottom
R305	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 3 Bottom
R306	RESISTOR CHIP RC12G 1% 21K5	5322 117 12492	B 3 Top
R307	RESISTOR CHIP TC50 1% 10K	4022 301 22071	A 4 Bottom
R308	RESISTOR CHIP RC12G 1% 21K5	5322 117 12492	B 3 Bottom
R309	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 3 Bottom
R310	RESISTOR CHIP TC50 1% 100K	4022 301 22311	B 3 Bottom
R311	RESISTOR CHIP RC12H 1% 31K6	5322 117 12466	B 3 Bottom
R312	RESISTOR CHIP RC12H 1% 34K8	5322 117 12467	C 3 Top
R321	RESISTOR CHIP RC12H 1% 681K	5322 117 12458	C 3 Top
R322	RESISTOR CHIP RC12H 1% 681K	5322 117 12458	C 3 Top
R323	RESISTOR CHIP RC12H 1% 34K8	5322 117 12467	B 3 Top
R324	RESISTOR CHIP RC12H 1% 215K	5322 117 12457	B 3 Top
R326	RESISTOR CHIP RC12H 1% 562K	5322 117 12468	C 3 Bottom
R327	RESISTOR CHIP RC12H 1% 562K	5322 117 12468	C 3 Top

Reference Designator	Description	Ordering Code	PCA Location
R331	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 4 Bottom
R333	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 3 Top
R337	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 3 Bottom
R339	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 3 Top
R342	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 3 Bottom
R352	RESISTOR CHIP RC12H 1% 5K11	5322 117 12469	A 1 Bottom
R353	RESISTOR CHIP RC12H 1% 1K	4822 117 11154	A 1 Bottom
R354	RESISTOR CHIP RC-02H 1% 261E	4822 051 52611	A 3 Bottom
R356	RESISTOR CHIP RC-02H 1% 261E	4822 051 52611	A 3 Bottom
R369	RESISTOR CHIP TC100 1% 13K3	4022 301 22101	C 3 Bottom
R371	RESISTOR CHIP RC12H 1% 0E	5322 117 12471	B 3 Bottom
R375	RESISTOR CHIP RC12H 1% 0E	5322 117 12471	C 5 Bottom
R376	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	C 3 Bottom
R377	RESISTOR CHIP RC12H 1% 1E	5322 117 12472	C 3 Bottom
R378	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	C 3 Top
R381	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	C 3 Top
R385	RESISTOR CHIP RC12H 1% 0E	5322 117 12471	B 4 Bottom
R390	RESISTOR CHIP RC12H 1% 464K	5322 117 12474	C 3 Bottom
R391	RESISTOR CHIP RC12H 1% 1K	4822 117 11154	C 3 Top
R392	RESISTOR CHIP RC12H 1% 4K22	5322 117 12476	C 3 Top
R393	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	D 3 Bottom
R394	RESISTOR CHIP RC12H 1% 1E	5322 117 12472	D 3 Bottom
R395	RESISTOR CHIP RC12H 1% 0E	5322 117 12471	D 3 Bottom
R396	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	D 3 Bottom
R398	RESISTOR CHIP RC12H 1% 1E	5322 117 12472	D 3 Bottom
R400	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 3 Top
R401	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 3 Top
R404	RESISTOR CHIP RC12H 1% 1E	5322 117 12472	A 3 Bottom
R405	RESISTOR CHIP RC12H 1% 1K	4822 117 11154	A 4 Bottom
R406	RESISTOR CHIP RC12H 1% 511E	5322 117 12451	A 4 Bottom
R407	RESISTOR CHIP RC12H 1% 3K16	5322 117 12465	A 4 Bottom
R408	RESISTOR CHIP RC11 2% 10M	4822 051 20106	A 3 Bottom
R409	RESISTOR CHIP RC12H 1% 26K1	5322 117 12448	A 3 Bottom
R410	RESISTOR CHIP RC12H 1% 68E1	5322 117 12454	A 3 Bottom

Reference Designator	Description	Ordering Code	PCA Location
R416	RESISTOR CHIP RC12H 1% 1E	5322 117 12472	B 5 Bottom
R417	RESISTOR CHIP RC12H 1% 1E	5322 117 12472	A 3 Bottom
R421	RESISTOR CHIP RC22H 1% 47E	2322 704 64709	A 4 Bottom
R422	RESISTOR CHIP RC22H 1% 47E	2322 704 64709	A 4 Bottom
R423	RESISTOR CHIP RC22H 1% 47E	2322 704 64709	A 4 Bottom
R424	RESISTOR CHIP RC22H 1% 47E	2322 704 64709	B 4 Bottom
R425	RESISTOR CHIP RC22H 1% 47E	2322 704 64709	A 4 Bottom
R426	RESISTOR CHIP RC22H 1% 47E	2322 704 64709	A 4 Bottom
R427	RESISTOR CHIP RC22H 1% 47E	2322 704 64709	A 3 Bottom
R428	RESISTOR CHIP RC22H 1% 47E	2322 704 64709	A 4 Bottom
R431	RESISTOR CHIP RC12H 1% 21K5	5322 117 12477	B 4 Bottom
R432	RESISTOR CHIP RC12H 1% 147K	5322 117 12478	B 4 Bottom
R433	RESISTOR CHIP RC12H 1% 147K	5322 117 12478	C 4 Bottom
R434	RESISTOR CHIP RC12H 1% 147K	5322 117 12478	C 4 Bottom
R436	RESISTOR CHIP RC12H 1% 26K1	5322 117 12448	B 4 Bottom
R438	RESISTOR CHIP RC12H 1% 147K	5322 117 12478	C 4 Bottom
R439	RESISTOR CHIP RC12H 1% 21K5	5322 117 12477	B 4 Bottom
R441	RESISTOR CHIP TC50 1% 21K5	4022 301 22151	C 4 Bottom
R442	RESISTOR CHIP RC12H 1% 1K47	5322 117 12479	B 4 Bottom
R443	RESISTOR CHIP TC100 1% 147E	4022 301 21631	B 3 Top
R444	RESISTOR CHIP TC100 1% 147E	4022 301 21631	B 3 Top
R450	RESISTOR CHIP TC50 1% 10K	4022 301 22071	C 3 Bottom
R451	RESISTOR CHIP TC50 1% 10K	4022 301 22071	C 3 Top
R454	RESISTOR CHIP RC12H 1% 1E	5322 117 12472	C 3 Bottom
R457	RESISTOR CHIP TC250 1% 1E	4022 301 21291	C 3 Bottom
R466	RESISTOR CHIP RC12H 1% 1E	5322 117 12472	B 5 Bottom
R470	RESISTOR CHIP RC12H 1% 0E	5322 117 12471	C 5 Bottom
R471	RESISTOR CHIP TC50 1% 1M	4022 301 22441	C 4 Bottom
R473	RESISTOR CHIP RC12H 1% 100E	4822 117 11373	C 3 Top
R474	RESISTOR CHIP RC12H 1% 100E	4822 117 11373	C 3 Top
R475	RESISTOR CHIP RC11 2A 0E	4022 301 21281	A 4 Bottom
R476	RESISTOR CHIP RC11 2A 0E	4022 301 21281	A 4 Bottom
R477	RESISTOR CHIP RC11 2A 0E	4022 301 21281	A 4 Bottom
R478	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 4 Bottom

Reference Designator	Description	Ordering Code	PCA Location
R479	RESISTOR CHIP RC12H 1% 51K1	5322 117 12462	B 4 Bottom
R480	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 4 Bottom
R481	RESISTOR CHIP TC50 1% 1M	4022 301 22441	C 4 Top
R482	RESISTOR CHIP TC100 1% 82E5	4022 301 21571	C 4 Top
R483	RESISTOR CHIP TC50 1% 1M	4022 301 22441	C 4 Top
R484	RESISTOR CHIP TC100 1% 511E	4022 302 21761	C 4 Top
R485	RESISTOR CHIP TC50 1% 10K	4022 301 22071	C 4 Bottom
R487	RESISTOR CHIP TC50 1% 100K	4022 301 22311	B 4 Bottom
R490	RESISTOR CHIP TC50 1% 10K	4022 301 22071	C 4 Bottom
R491	RESISTOR CHIP TC100 1% 42K2	4022 301 22221	C 4 Top
R492	RESISTOR CHIP TC50 1% 1K	4022 301 21831	B 4 Bottom
R493	RESISTOR CHIP TC50 1% 100K	4022 301 22311	C 4 Bottom
R494	RESISTOR CHIP TC50 1% 100K	4022 301 22311	C 4 Bottom
R495	RESISTOR CHIP RC12H 1% 3K16	5322 117 12465	A 3 Bottom
R496	RESISTOR CHIP RC12H 1% 3K16	5322 117 12465	A 3 Bottom
R497	RESISTOR CHIP RC12H 1% 0E	5322 117 12471	C 4 Bottom
R498	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 4 Bottom
R501	RESISTOR CHIP LRC01 5% 0E1	5322 117 11759	D 3 Bottom
R502	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	D 4 Bottom
R503	RESISTOR CHIP RC12H 1% 10E	5322 117 12464	D 5 Bottom
R504	RES FRC01 1206 5% 1E	4822 117 11151	B 5 Bottom
R506	RES FRC01 1206 5% 1E	4822 117 11151	B 5 Bottom
R507	RES FRC01 1206 5% 1E	4822 117 11151	B 5 Bottom
R508	RESISTOR CHIP TC50 1% 10K	4022 301 22071	C 4 Bottom
R509	RESISTOR CHIP RC12H 1% 46E4	5322 117 12463	D 5 Bottom
R512	RESISTOR CHIP RC12H 1% 2K87	5322 117 12608	D 5 Bottom
R513	RESISTOR CHIP RC12H 1% 26K1	5322 117 12448	D 5 Bottom
R514	RESISTOR CHIP TC100 1% 3K16	4022 301 21951	D 5 Bottom
R515	RESISTOR CHIP TC100 1% 23K7	4022 301 22161	D 5 Bottom
R524	RESISTOR CHIP RC12H 1% 100E	4822 117 11373	D 5 Bottom
R527	RESISTOR CHIP RC12H 1% 147E	5322 117 12482	D 3 Bottom
R528	RESISTOR CHIP RC12H 1% 34K8	5322 117 12467	D 4 Bottom
R529	RESISTOR CHIP RC12H 1% 261K	5322 117 12617	D 3 Bottom

Reference Designator	Description	Ordering Code	PCA Location
R531	RESISTOR CHIP TC50 1% 100K	4022 301 22311	C 4 Bottom
R532	SMD RES 100E 1% TC100 0805	4022 301 21591	C 4 Bottom
R534	RESISTOR CHIP RC12H 1% 1K47	5322 117 12479	D 4 Bottom
R535	RESISTOR CHIP RC12H 1% 51K1	5322 117 12462	D 4 Bottom
R550	RESISTOR CHIP RC12H 1% 348E	5322 117 12456	D 5 Bottom
R551	RESISTOR CHIP LRC01 5% 0E1	5322 117 11759	C 5 Bottom
R552	RESISTOR CHIP TC50 1% 10K	4022 301 22071	D 5 Bottom
R553	RESISTOR CHIP RC12H 1% 4K22	5322 117 12476	D 5 Bottom
R554	RESISTOR CHIP RC12H 1% 26K1	5322 117 12448	D 5 Bottom
R558	RESISTOR CHIP RC12H 1% 31K6	5322 117 12466	D 5 Bottom
R559	RESISTOR CHIP RC12H 1% 5K11	5322 117 12469	D 5 Bottom
R563	RESISTOR CHIP TC50 1% 100K	4022 301 22311	D 5 Bottom
R564	RESISTOR CHIP TC50 1% 100K	4022 301 22311	D 5 Bottom
R565	RESISTOR CHIP TC50 1% 100K	4022 301 22311	D 5 Bottom
R570	RESISTOR CHIP TC50 1% 100K	4022 301 22311	C 5 Bottom
R580	RESISTOR CHIP LRC01 5% 0E33	5322 117 11725	D 4 Bottom
R591	RESISTOR CHIP RC12H 1% 2K15	5322 117 12452	B 4 Bottom
R600	RESISTOR CHIP RC12H 1% 5K11	5322 117 12469	B 5 Bottom
R601	RESISTOR CHIP TC100 1% 68E1	4022 301 21551	A 5 Bottom
R602	RESISTOR CHIP TC50 1% 10K	4022 301 22071	B 5 Bottom
R603	RESISTOR CHIP TC50 1% 100K	4022 301 22311	B 4 Bottom
R604	RESISTOR CHIP RC12H 1% 1K	4822 117 11154	B 5 Bottom
R605	SMD RES 10 K 1% TC50 0805	4022 301 22071	A 4 Bottom
R606	SMD RES 6K19 1% TC50 0805	4022 301 22021	A 4 Bottom
T552	BACKLIGHT TRANSFORMER PT73458	5322 146 10447	C 5 Top
T600	SMD TRANSFORMER 678XN-1081 TOK	5322 146 10634	A 5 Top
V171 *	PNP/NPN TR.PAIR BCV65	5322 130 10762	A 3 Bottom
V172 *	PNP/NPN TR.PAIR BCV65	5322 130 10762	C 3 Bottom
V174 *	PNP/NPN TR.PAIR BCV65	5322 130 10762	A 3 Bottom

Reference Designator	Description	Ordering Code	PCA Location
V301 *	PREC.VOLT.REF. LM4041CIM-1.2	5322 209 14852	2X4 pin DIL
V302 *	PREC.VOLT.REF. LM4041CIM-1.2 3X	4022 304 10571	B 3 Bottom, Transistor shape
V353 *	VOLT REG DIODE BZD27-C7V5 PEL	4822 130 82522	A 1 Bottom
V354 *	VOLT REG DIODE BZD27-C7V5 PEL	4822 130 82522	A 1 Bottom
V356 *	LF TRANSISTOR BC858C PEL	4822 130 42513	A 3 Bottom
V358 *	LF TRANSISTOR BC868 PEL	5322 130 61569	A 2 Bottom
V359 *	LF TRANSISTOR BC868 PEL	5322 130 61569	A 2 Bottom
V395 *	LF TRANSISTOR BC848C PEL	5322 130 42136	C 3 Bottom
V401 *	N-CHAN FET BSN20 PEL	5322 130 63289	A 4 Top
V402 *	P-CHAN. MOSFET BSS84 PEL	5322 130 10669	A 4 Top
V403 *	N-CHAN FET BSN20 PEL	5322 130 63289	V403 A 4 Bottom
V471 *	SCHOTTKY DIODE BAT74	9337 422 90215	V471 C 4 Top
V495 *	P-CHAN. MOSFET BSS84 PEL	5322 130 10669	A 3 Bottom
V501 *	SCHOTTKY DIODE MBRS340T3 MOT	5322 130 10674	D 3 Bottom
V503 *	SCHOTTKY DIODE MBRS340T3 MOT	5322 130 10674	D 4 Bottom
V504 *	SCHOTTKY DIODE MBRS340T3 MOT	5322 130 10674	D 4 Bottom
V506 *	POWER TMOS FET MTD5P06ET4 MOT	5322 130 10671	D 4 Bottom
V550 *	RECT DIODE BYD77A	5322 130 10763	D 5 Bottom
V551 *	RECT DIODE BYD77A	5322 130 10763	C 5 Bottom
V554 *	N-CHAN MOSFET 2SK974STR HIT	5322 130 62921	C 5 Bottom
V555 *	RECT DIODE BYD77A	5322 130 10763	C 5 Bottom
V561 *	SCHOTTKY DIODE MBRS340T3 MOT	5322 130 10674	C 5 Bottom
V562 *	SCHOTTKY DIODE MBRS340T3 MOT	5322 130 10674	C 5 Bottom
V563 *	SCHOTTKY DIODE MBRS340T3 MOT	5322 130 10674	B 5 Bottom
V564 *	SCHOTTKY DIODE MBRS1100T3 MOT	5322 130 10675	B 5 Bottom
V565 *	LF TRANSISTOR BC848C PEL	5322 130 42136	D 5 Bottom
V566 *	LF TRANSISTOR BC848C PEL	5322 130 42136	D 5 Bottom
V567 *	SCHOTTKY DIODE MBRS340T3 MOT	5322 130 10674	C 5 Bottom
V569 *	LF TRANSISTOR BC869 PEL	4822 130 60142	D 5 Bottom
V600 *	TMOS P-CH FET MMSF3P03HD MOT	5322 130 10672	A 5 Bottom
V601 *	TMOS N-CH FET MMDF3N04HD MOT	4022 304 10221	A 5 Bottom
V602 *	SCHOTTKY DIODE MBRS340T3 MOT	5322 130 10674	A 5 Bottom
V603 *	SIL DIODE BAS16 PEL	5322 130 31928	B 4 Top
V604 *	N-CHAN FET BSN20 PEL	5322 130 63289	B 5 Bottom

Reference Designator	Description	Ordering Code	PCA Location
V605 *	LF TRANSISTOR BC858C PEL	4822 130 42513	B 5 Bottom
X452	FLEX-PRINT CONNECTOR 15-P FCN	5322 265 10725	A 4 Top
X453	FLEX-PRINT CONNECTOR 21-P FCN	5322 265 10726	A 3 Top
X501	DC POWER JACK HEC0739-01-010	4822 267 30431	D 4 Top
X503	MALE HEADER 2MM 6-P DBL RT.ANG	5322 267 10501	A 5 Top
X601	MALE HEADER 7-P SNG RT.ANG	5322 267 10502	A 4 Top
Z501	EMI-FILTER 50V 10A MUR	5322 156 11139	D 3 Top

8.6 Accessory Replacement Parts

Black ground lead for STL120 5322 320 11354

8.7 Service Tools

Power adapter cable to check supply current 5322 320 11707

Chapter 9
Circuit Diagrams

Title	Page

9.1 Introduction

This chapter contains all circuit diagrams and PCA drawings of the test tool. There are no serviceable parts on the LCD unit. Therefore no circuit diagrams and drawings of the LCD unit are provided.

Referring signals from one place to another in the circuit diagrams is done in the following way:

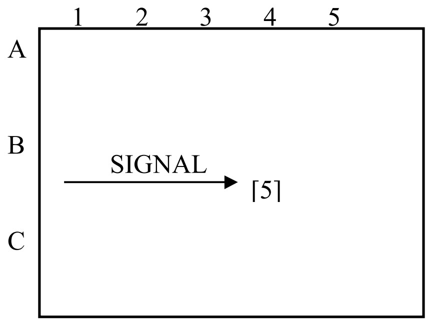


Figure 9.1 Circuit Diagram 1

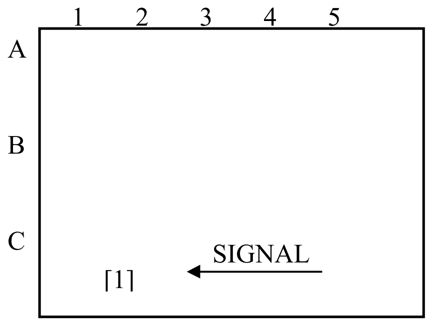


Figure 9.5 Circuit diagram 5

The line SIGNAL on circuit diagram 1 [1], is connected to the line SIGNAL on circuit diagram 5 [5].

If the signal is referred to a location on the same circuit diagram, the circuit diagram number is omitted.

9.2 Schematic Diagrams

Where to find parts on the Main PCA assembly drawings is listed for each component in the last column of the List of Main PCA parts in Chapter 8.5.
For each component the location (e.g. C 4) is given and also if the component is located on the Top Side of the PCA, or on the Bottom Side. On the Top Side the large components are located; on the Bottom Side the Surface Mounted Devices (SMD's)..

B402 C 4 Top indicates that part B402 can be found in:

location C4 on the Main PCA Top Side 1 drawing.

Measuring points are all on the Top Side of the Main PCA and are listed below.

MS401 A 3 Top	MS445 A 5 Top	TP451 C 4 Top	TP499 B 4 Top
MS402 A 3 Top	MS453 A 4 Top	TP452 C 4 Top	TP501 D 5 Top
MS403 A 3 Top	MS454 A 4 Top	TP453 C 4 Top	TP502 D 5 Top
MS404 A 3 Top		TP454 C 4 Top	TP503 D 4 Top
MS405 A 3 Top	TP151 C 3 Top	TP455 C 4 Top	TP504 D 5 Top
MS406 A 3 Top	TP152 B 3 Top	TP456 C 5 Top	TP521 D 3 Top
MS408 A 3 Top	TP153 B 3 Top	TP457 C 4 Top	TP522 D 4 Top
MS409 A 3 Top	TP154 B 3 Top	TP471 C 3 Top	TP526 C 4 Top
MS410 A 3 Top	TP156 B 3 Top	TP472 C 3 Top	TP527 D 4 Top
MS411 A 3 Top	TP251 C 3 Top	TP473 B 5 Top	TP528 C 5 Top
MS412 A 3 Top	TP252 C 2 Top	TP474 C 4 Top	TP529 D 5 Top
MS413 A 3 Top	TP253 C 4 Top	TP475 C 4 Top	TP531 D 4 Top
MS414 A 3 Top	TP254 C 3 Top	TP476 C 4 Top	TP534 C 4 Top
MS415 A 3 Top	TP256 C 3 Top	TP477 B 4 Top	TP536 C 4 Top
MS416 A 3 Top	TP301 C 3 Top	TP478 B 4 Top	TP537 C 4 Top
MS417 A 3 Top	TP302 C 3 Top	TP479 C 4 Top	TP551 C 5 Top
MS418 A 3 Top	TP303 C 3 Top	TP480 C 4 Top	TP552 C 5 Top
MS419 A 4 Top	TP304 C 3 Top	TP481 C 4 Top	TP561 D 4 Top
MS420 A 4 Top	TP306 D 4 Top	TP482 B 4 Top	TP567 C 5 Top
MS421 A 4 Top	TP307 D 4 Top	TP483 B 4 Top	TP571 D 4 Top
MS422 A 4 Top	TP308 C 3 Top	TP484 C 4 Top	TP572 A 3 Top
MS431 A 4 Top	TP310 B 3 Top	TP485 C 4 Top	TP573 B 5 Top
MS432 A 4 Top	TP311 C 3 Top	TP486 C 4 Top	TP574 C 5 Top
MS433 A 4 Top	TP321 C 3 Top	TP487 B 4 Top	TP577 D 5 Top
MS434 A 4 Top	TP322 C 3 Top	TP488 C 4 Top	TP591 C 5 Top
MS435 A 4 Top	TP331 B 3 Top	TP489 C 5 Top	TP592 C 5 Top
MS436 A 4 Top	TP332 B 3 Top	TP490 C 5 Top	TP593 C 5 Top
MS437 A 4 Top	TP336 B 3 Top	TP491 C 5 Top	TP600 B 5 Top
MS438 A 4 Top	TP338 B 3 Top	TP492 C 5 Top	TP601 A 5 Top
MS439 A 4 Top	TP431 B 3 Top	TP493 C 5 Top	TP602 A 5 Top
MS440 A 4 Top	TP432 B 3 Top	TP494 B 4 Top	TP603 A 5 Top
MS441 A 4 Top	TP433 C 3 Top	TP495 A 3 Top	TP604 B 4 Top
MS442 A 5 Top	TP436 B 3 Top	TP496 A 3 Top	TP605 B 5 Top
MS443 A 5 Top	TP438 B 3 Top	TP497 B 4 Top	
MS444 A 5 Top	TP450 C 4 Top	TP498 B 4 Top	

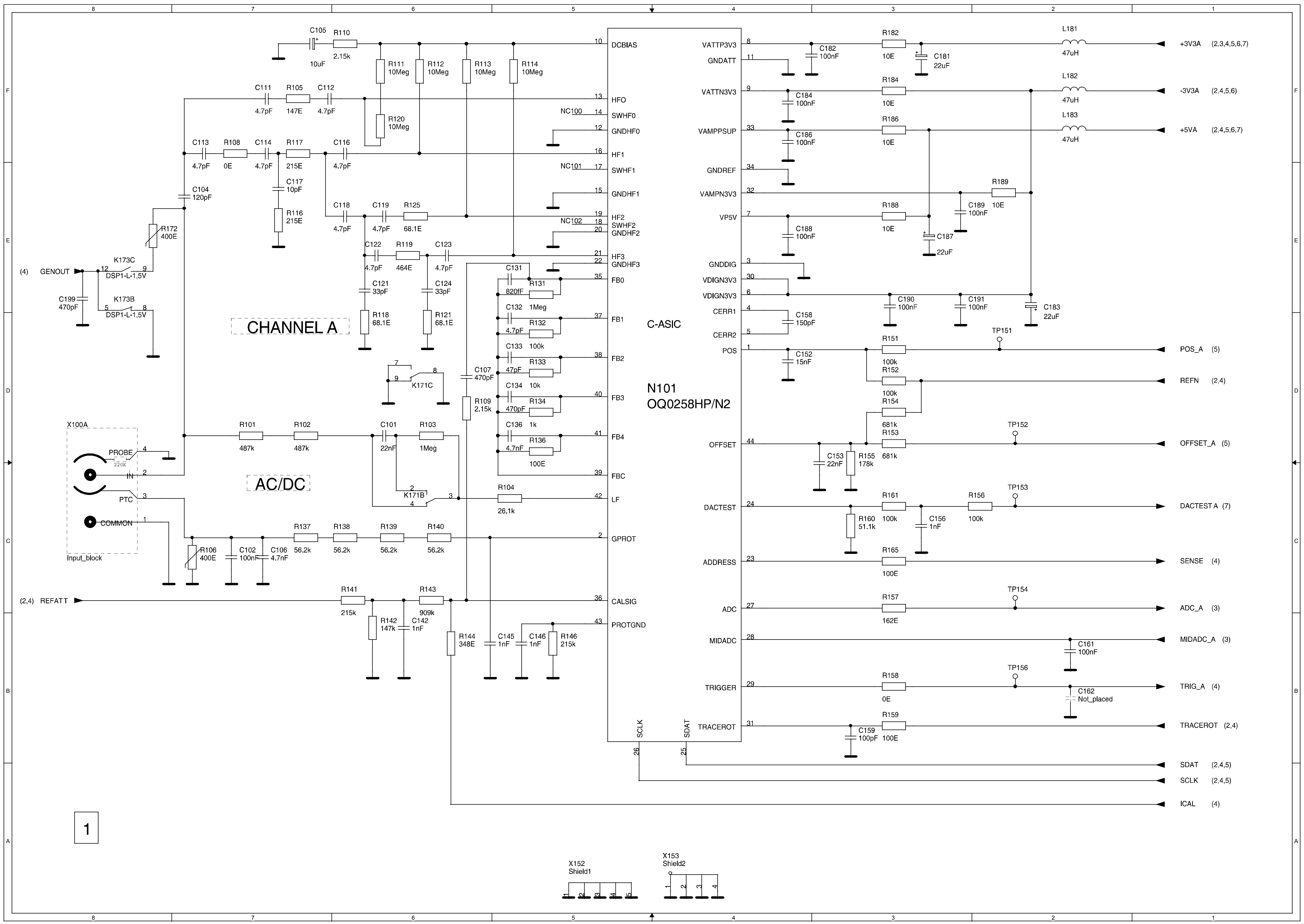


Figure 9-1. Circuit Diagram 1, Channel A Circuit

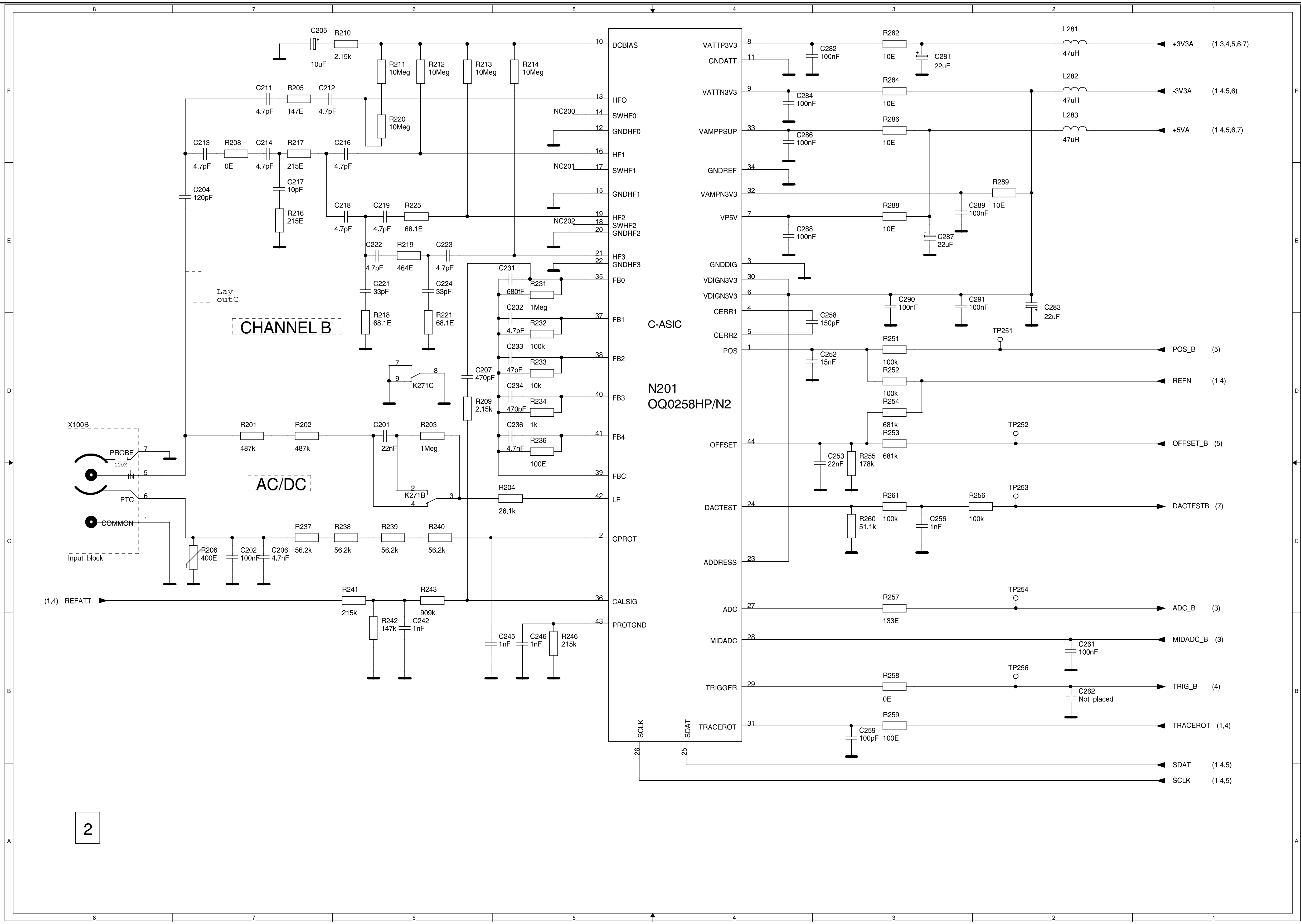


Figure 9-2. Circuit Diagram 2, Channel B Circuit

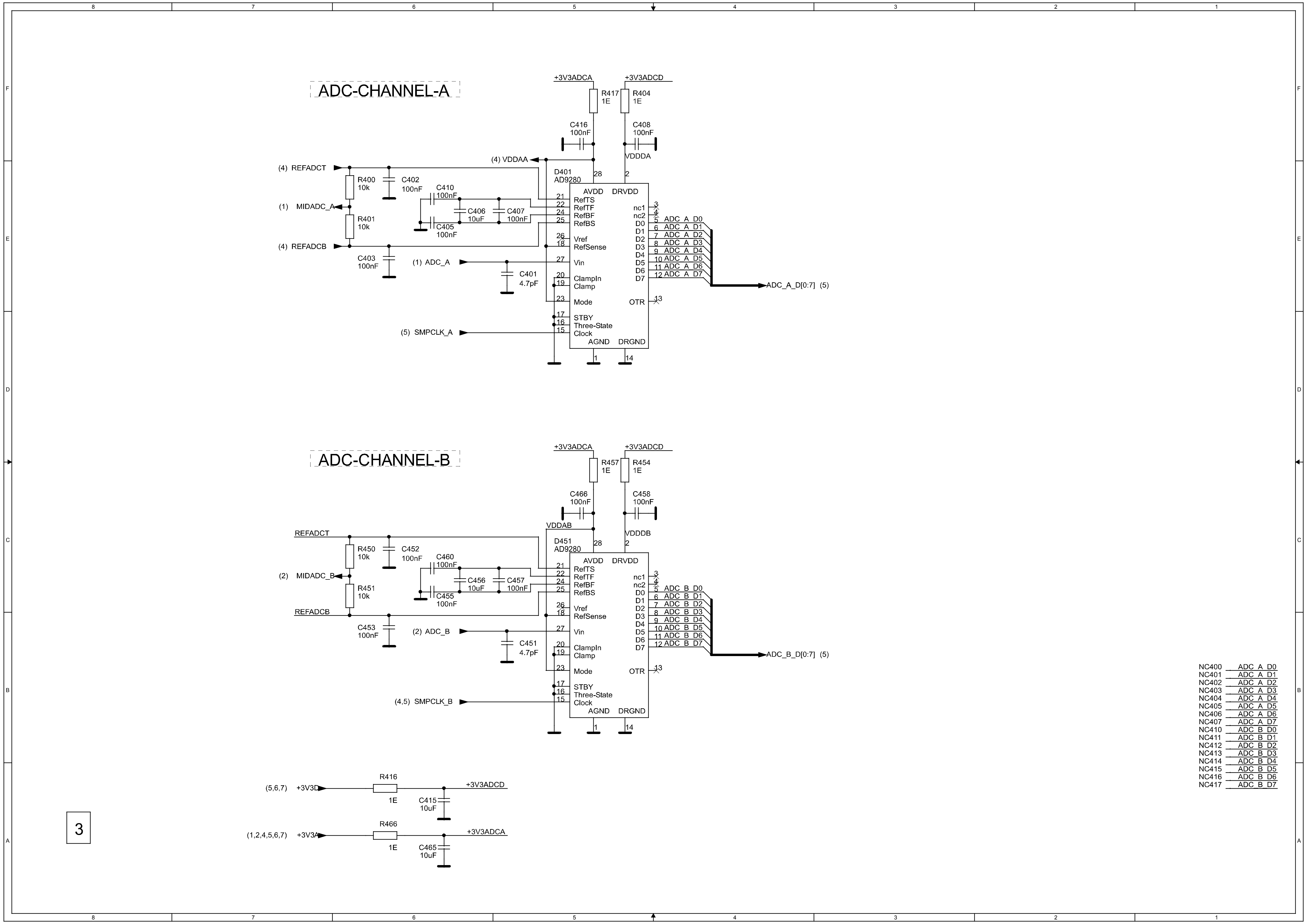


Figure 9-3. Circuit Diagram 3, Analog to Digital Conversion

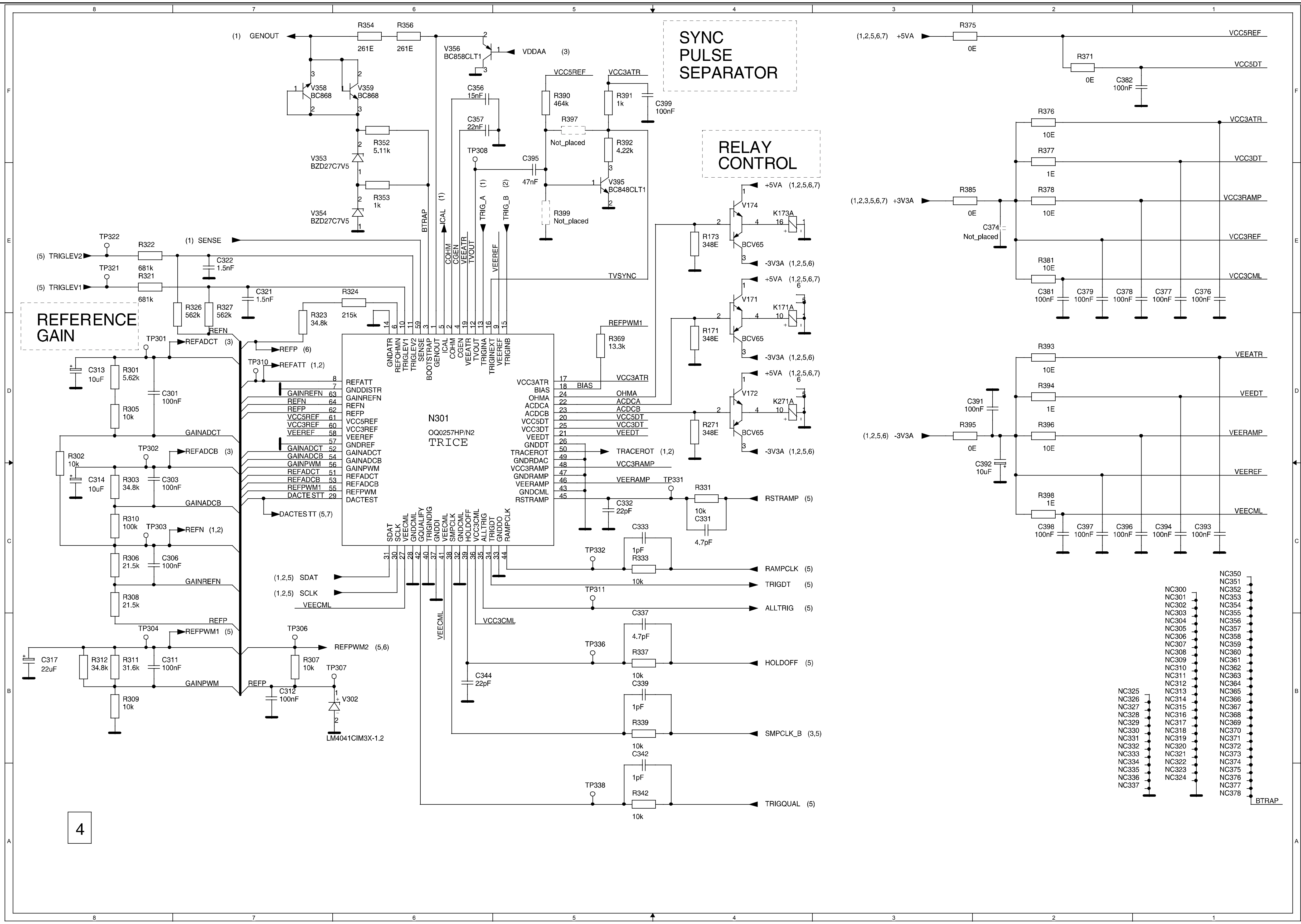


Figure 9-4. Circuit Diagram 4, Trigger Circuit

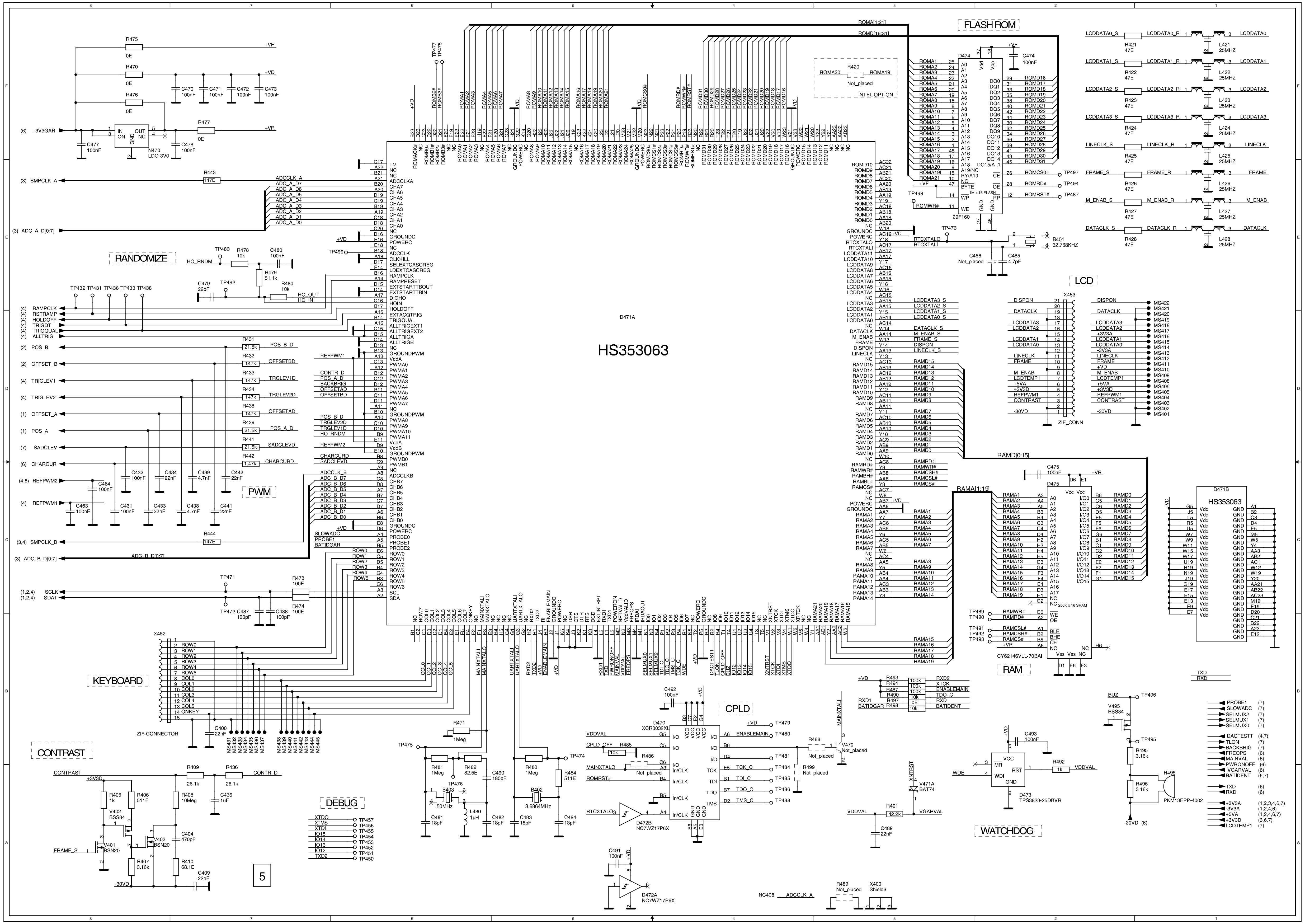


Figure 9-5. Circuit Diagram 5, Digital Circuit

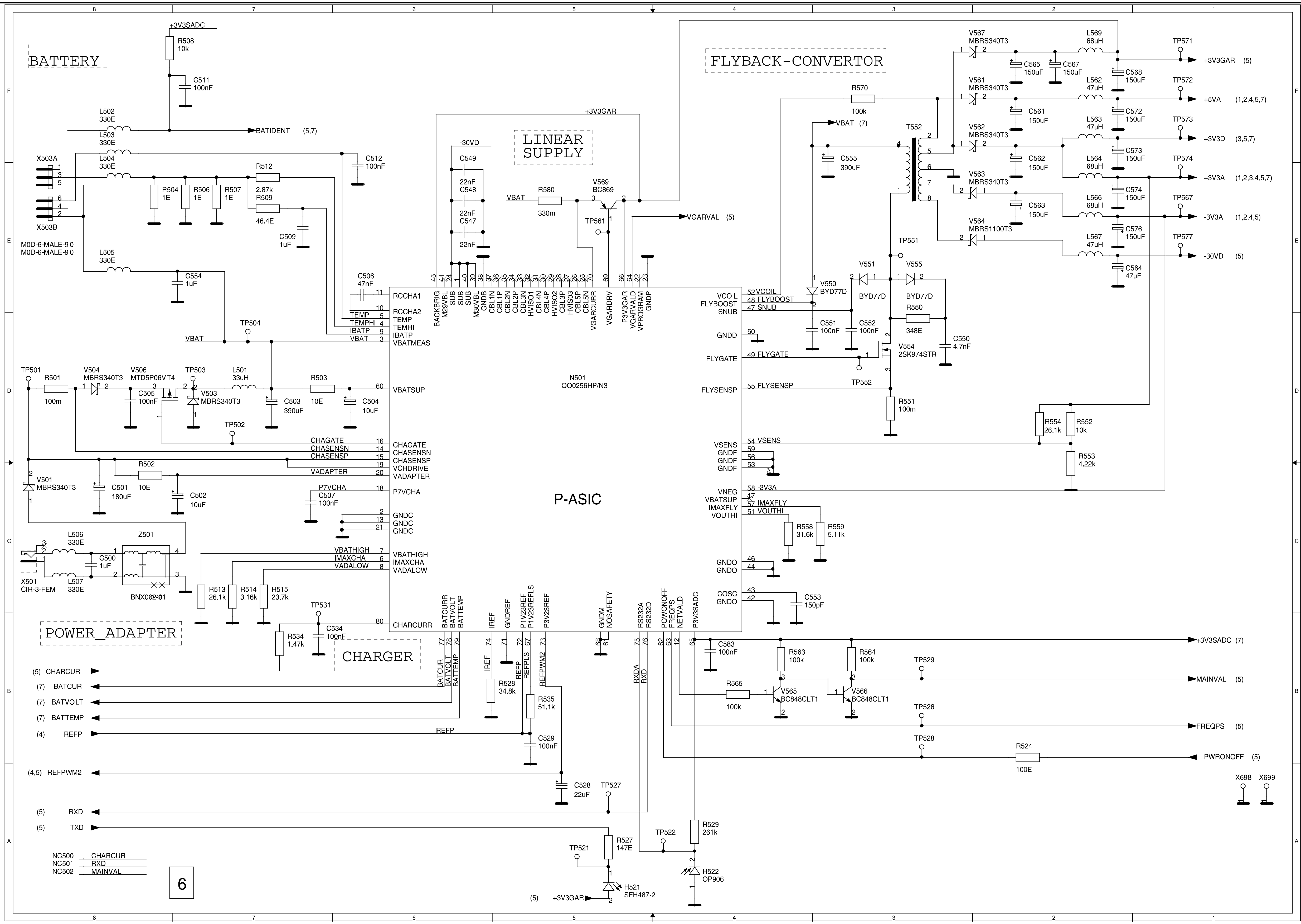


Figure 9-6. Circuit Diagram 6, Power Circuit

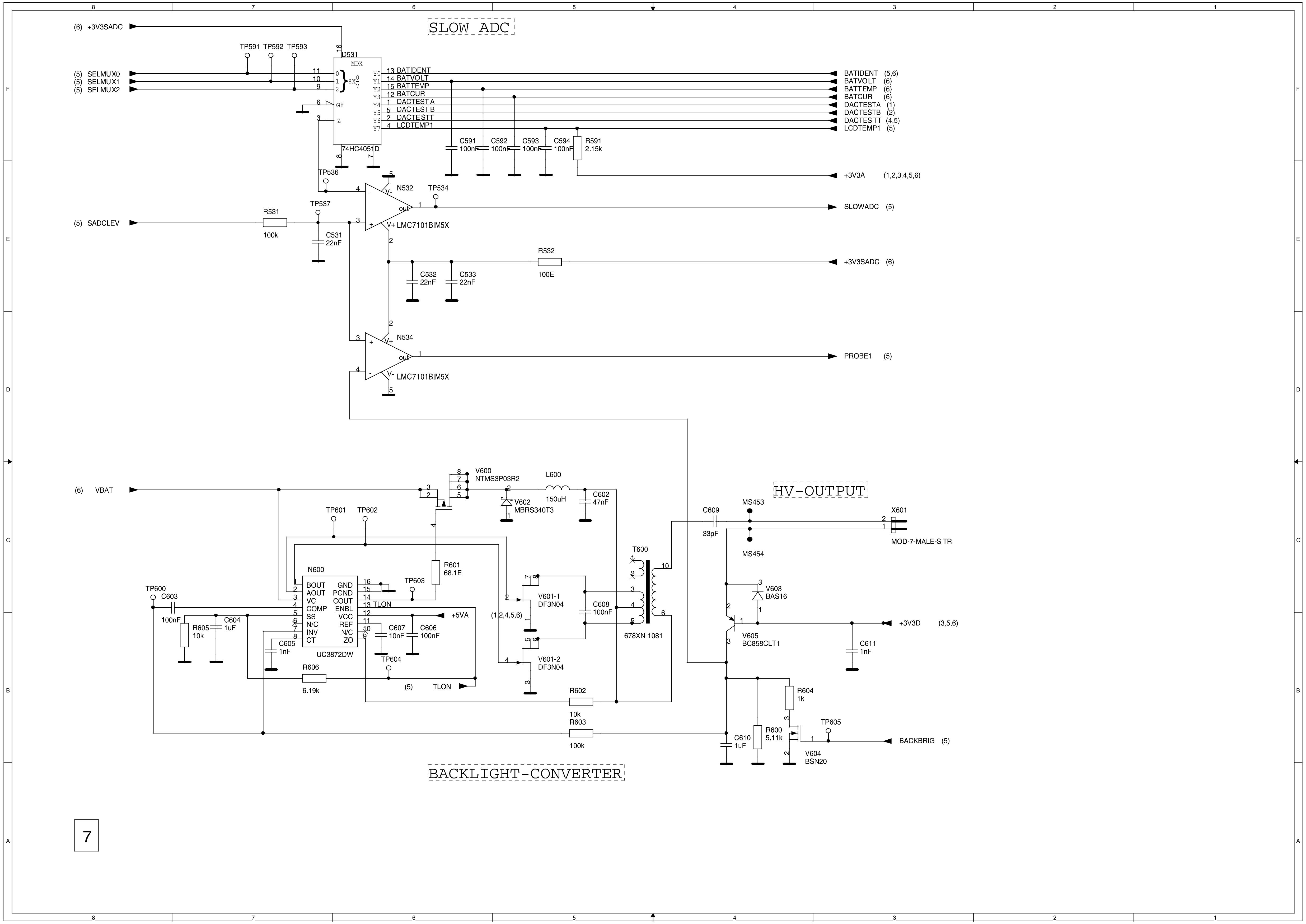


Figure 9-7. Circuit Diagram 7, Slow ADC / Backlight Converter

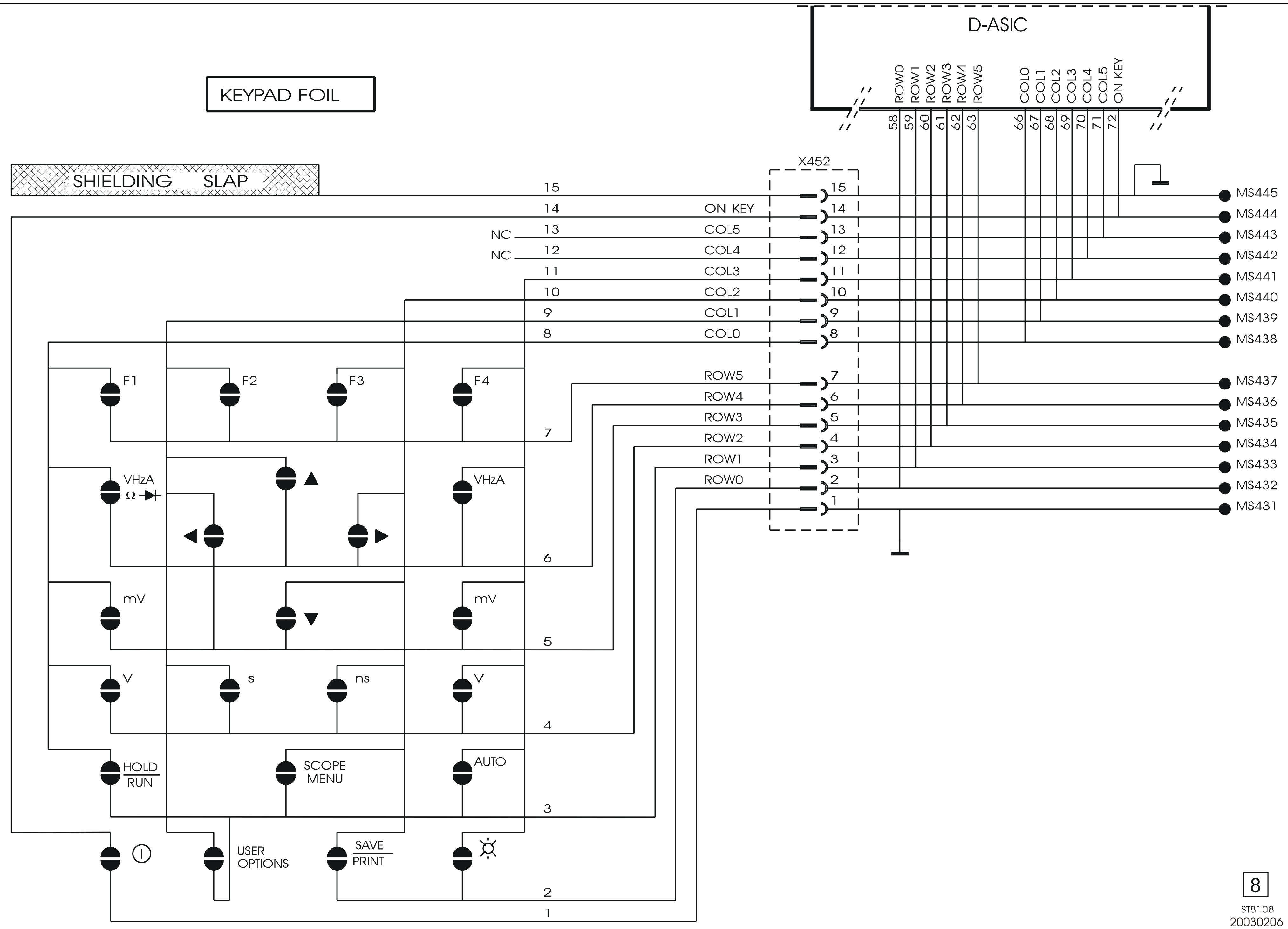


Figure 9-8. Circuit Diagram 8, Keyboard Circuit

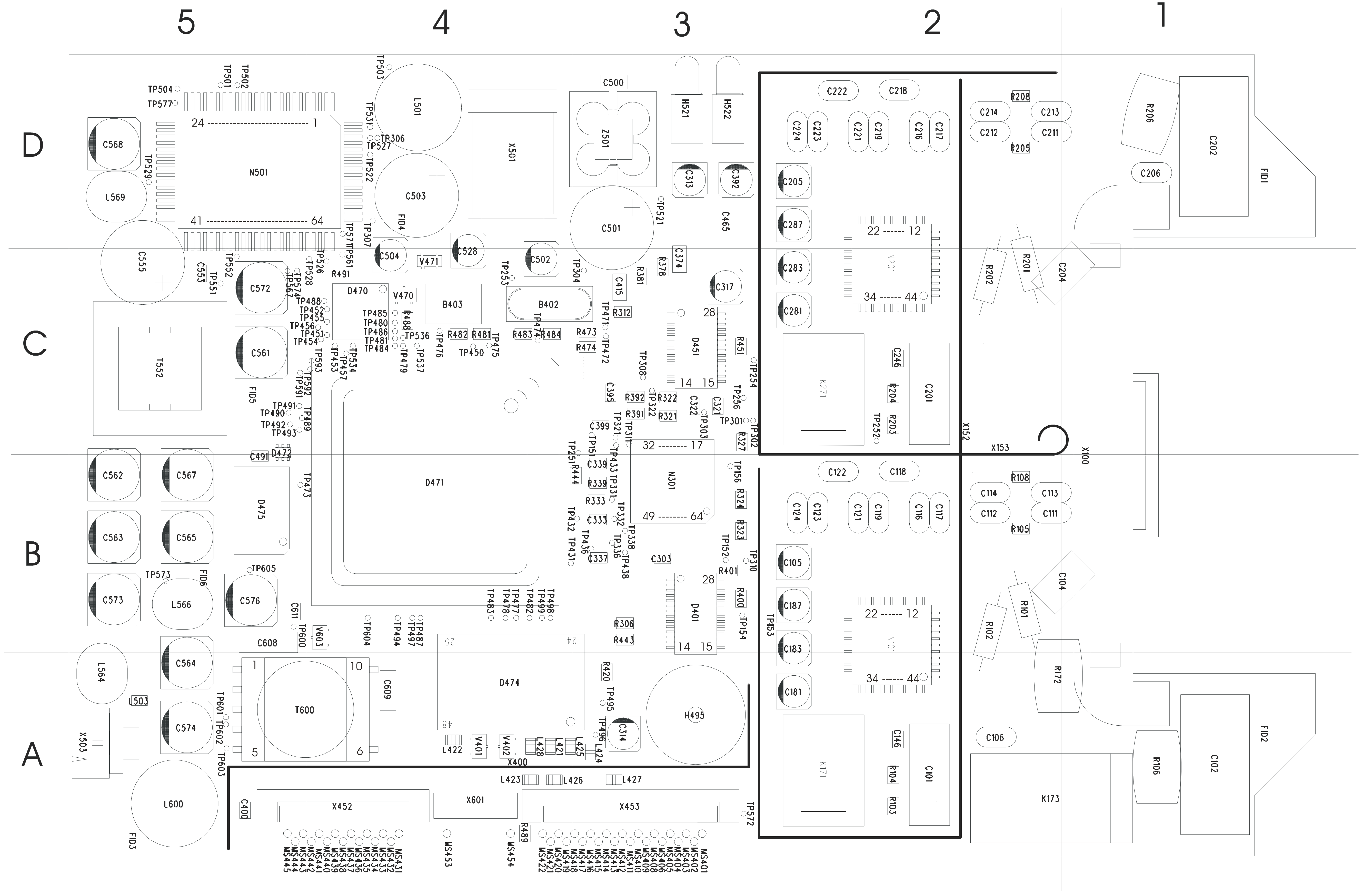


Figure 9-9. Main PCA, Large Component Side

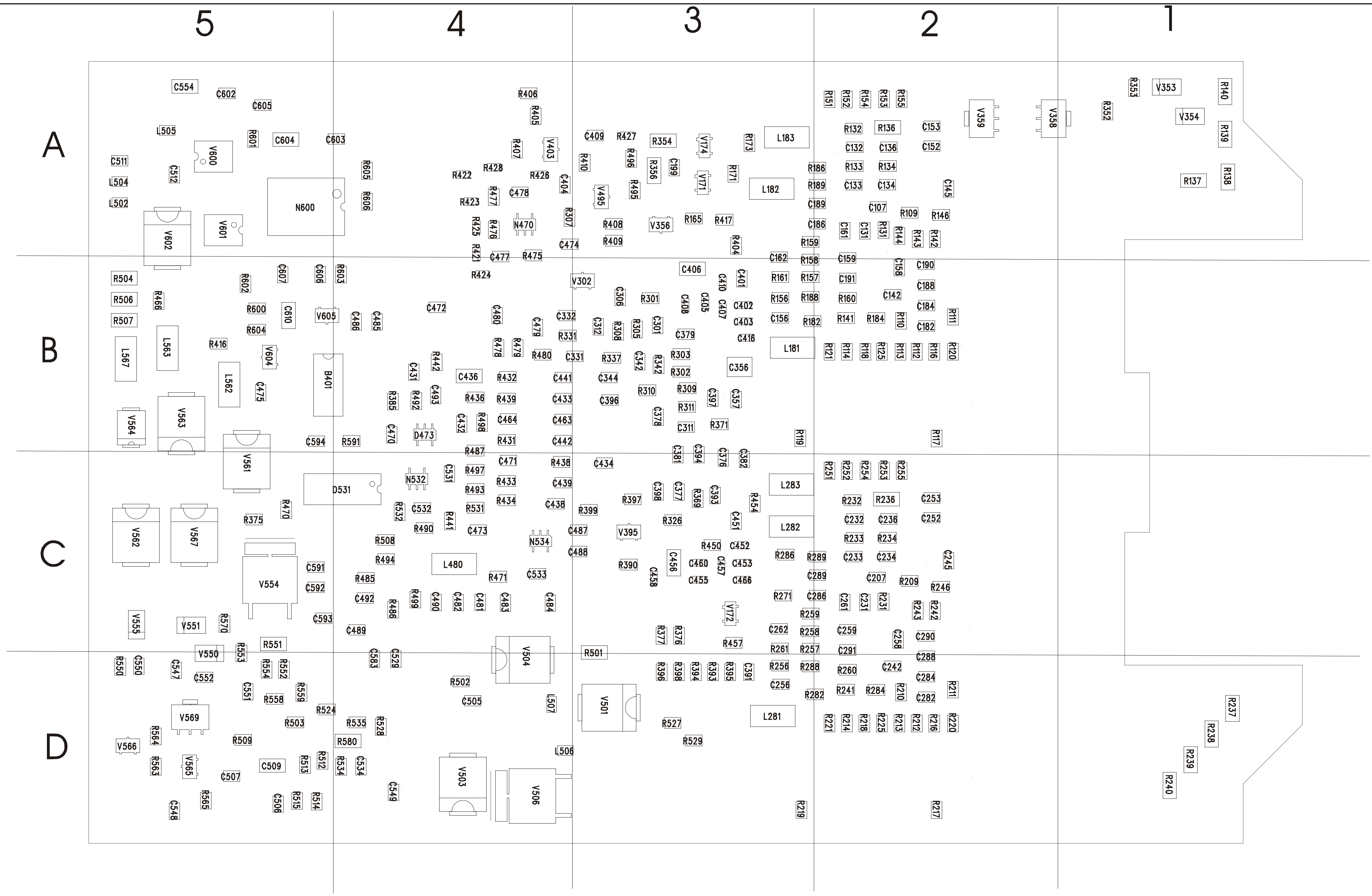


Figure 9-10. Main PCA, Small Component (SMD) Side

Chapter 10
Modifications

Title	Page

10.1 Software modifications

Changes and improvements made to the test tool software (firmware) are identified by incrementing the software version number. These changes are documented on a supplemental change/errata sheet which, when applicable, is included with the manual.

To display the software version, proceed as follows:

1. Press USER OPTIONS to open the USER OPTIONS menu.
2. Press F3 to show the VERSION&CALIBRATION screen (see Figure 5.1 in Section 5).
3. Press F4 to return to normal mode.

The first software release suitable for both Fluke 123 and Fluke 124 is V02.00. This release is still valid at the printing date of this Service Manual.

10.2 Hardware modifications

Changes and improvements made to the test tool hardware are identified by incrementing the revision number of the Main PCA. The revision number is printed on a sticker, see the example below. The sticker is placed on D-ASIC D471, on the Main PCA.

This example of the Main PCA revision number sticker indicates revision 1. →

1		

The following revisions have been released:

Revision 08

Revision number of first deliveries.